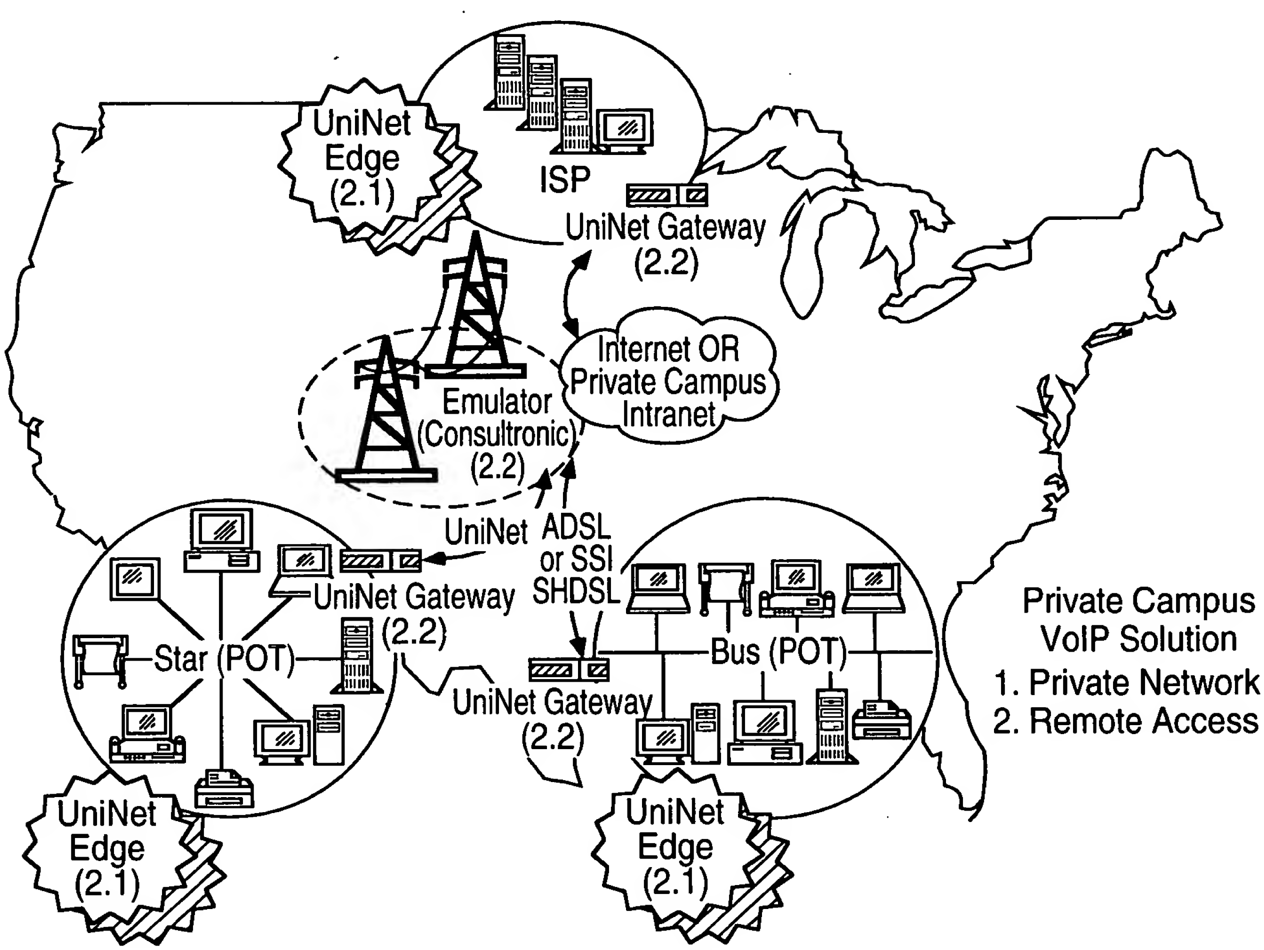


FIG. 1

Universal Intelligence Network (UniNet™)

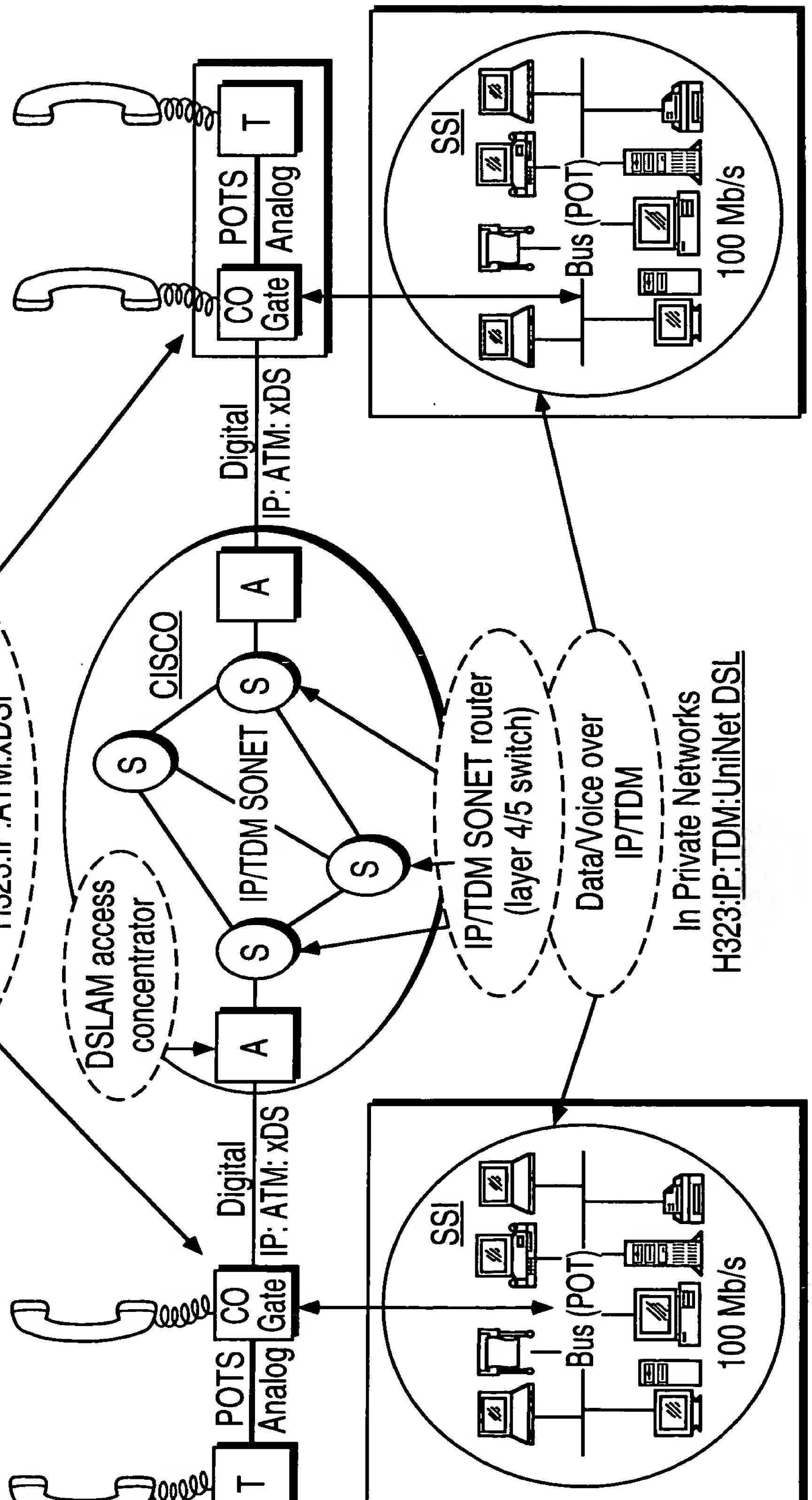


FIG. 2

Private UniNet™ Networks

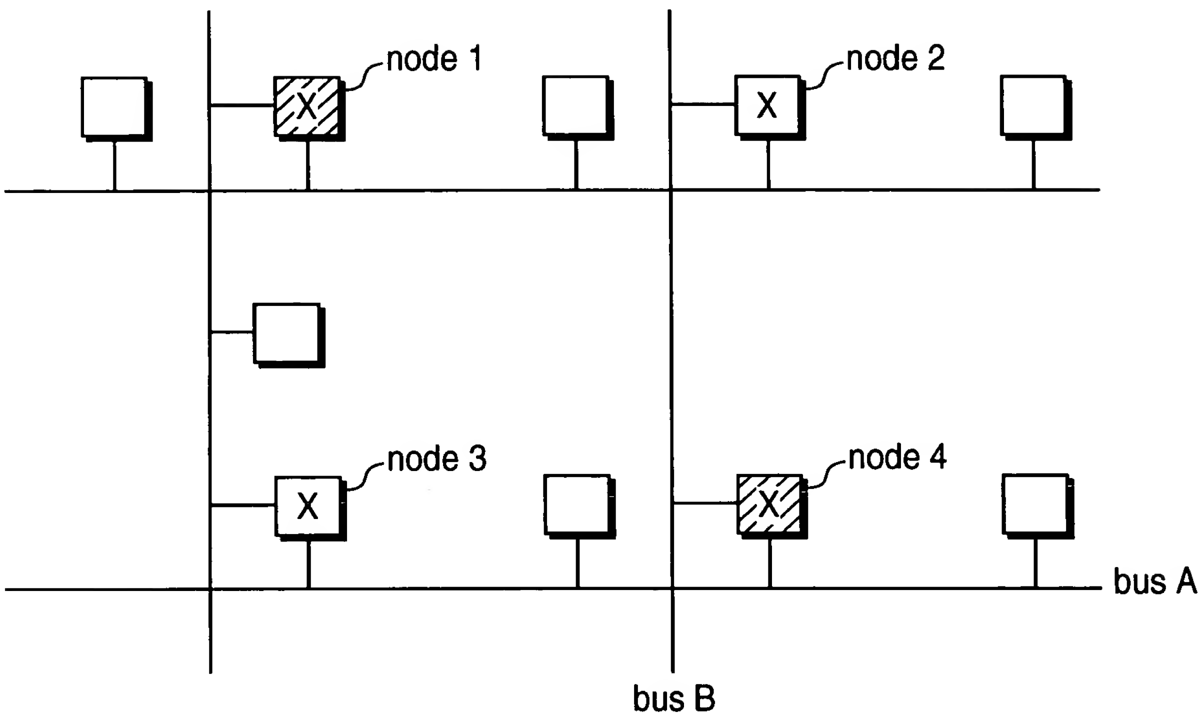


FIG. 3

UniNet nodes interconnected in a mesh structure

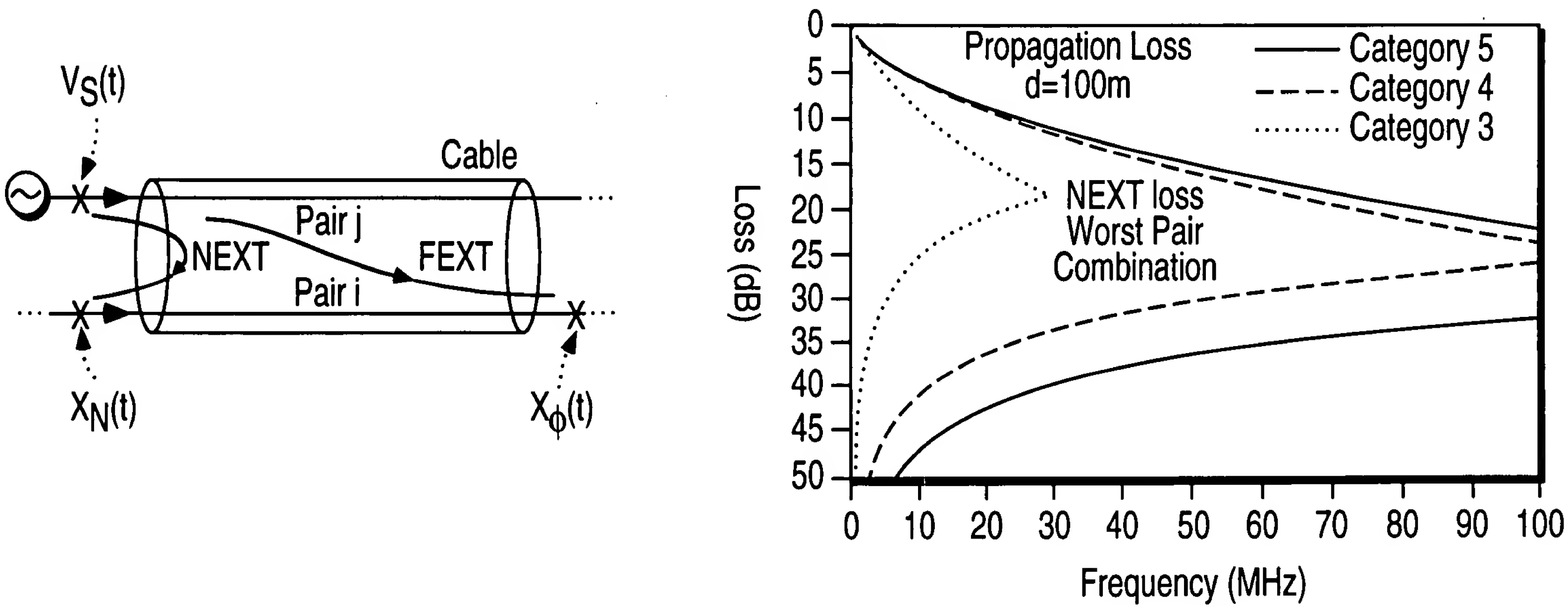


FIG. 4

Typical Near End and Far End Cross-talks Noise Environment

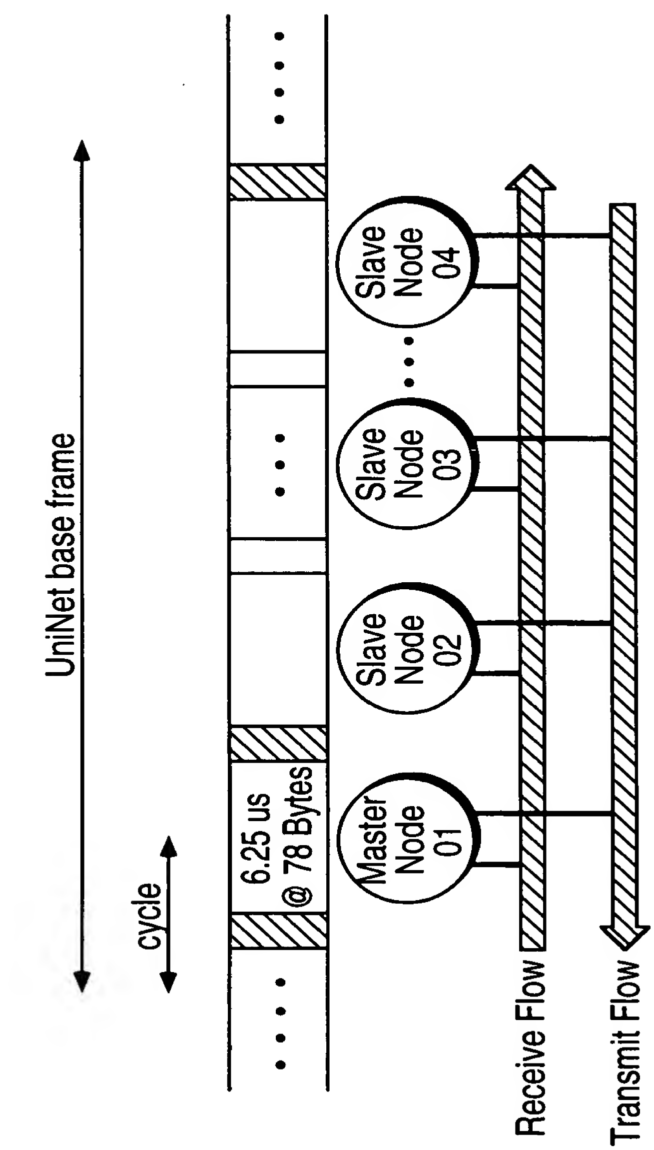


FIG. 5

TDM Transmit and Receive Flow cycles

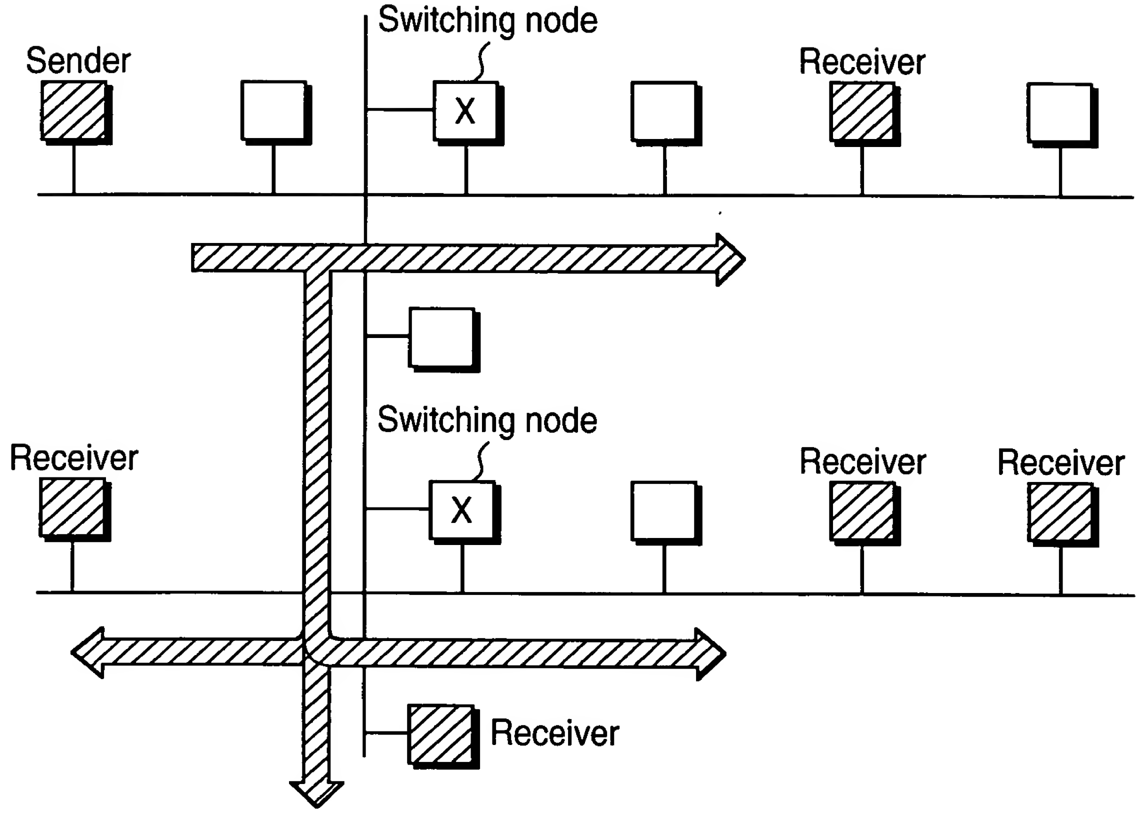


FIG. 6

A UniNet Multicast Group

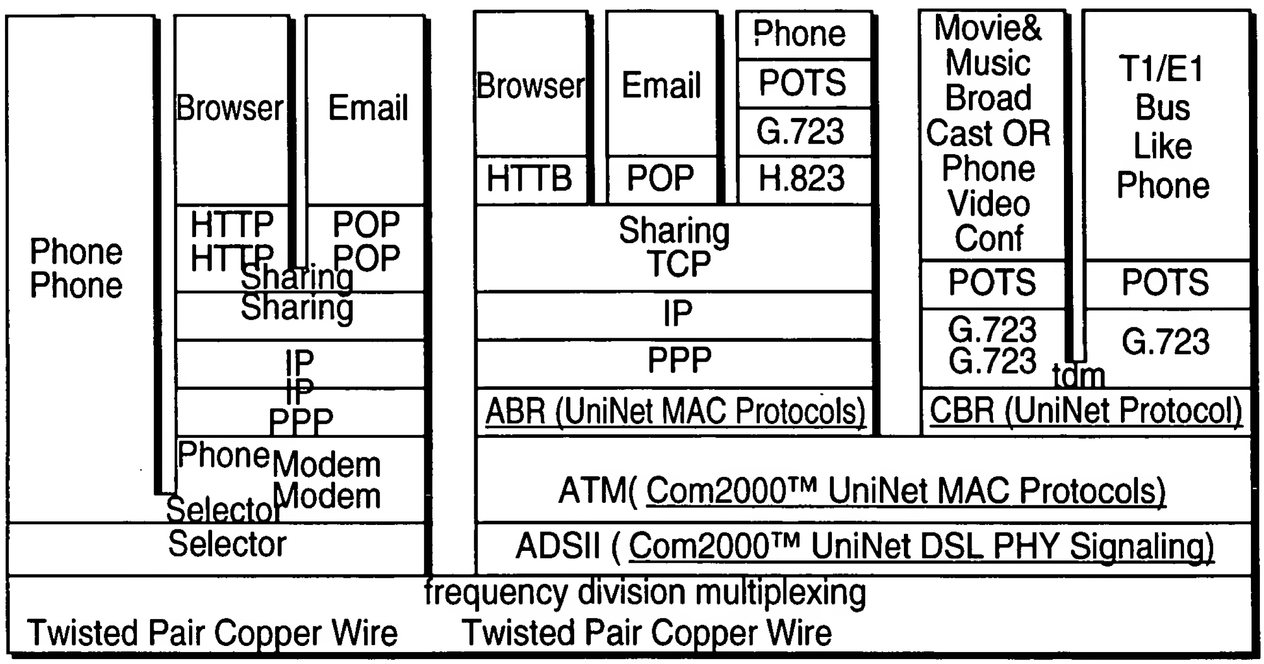


FIG. 7

UniNet Network over Plain Old Telephone Systems (POTS)

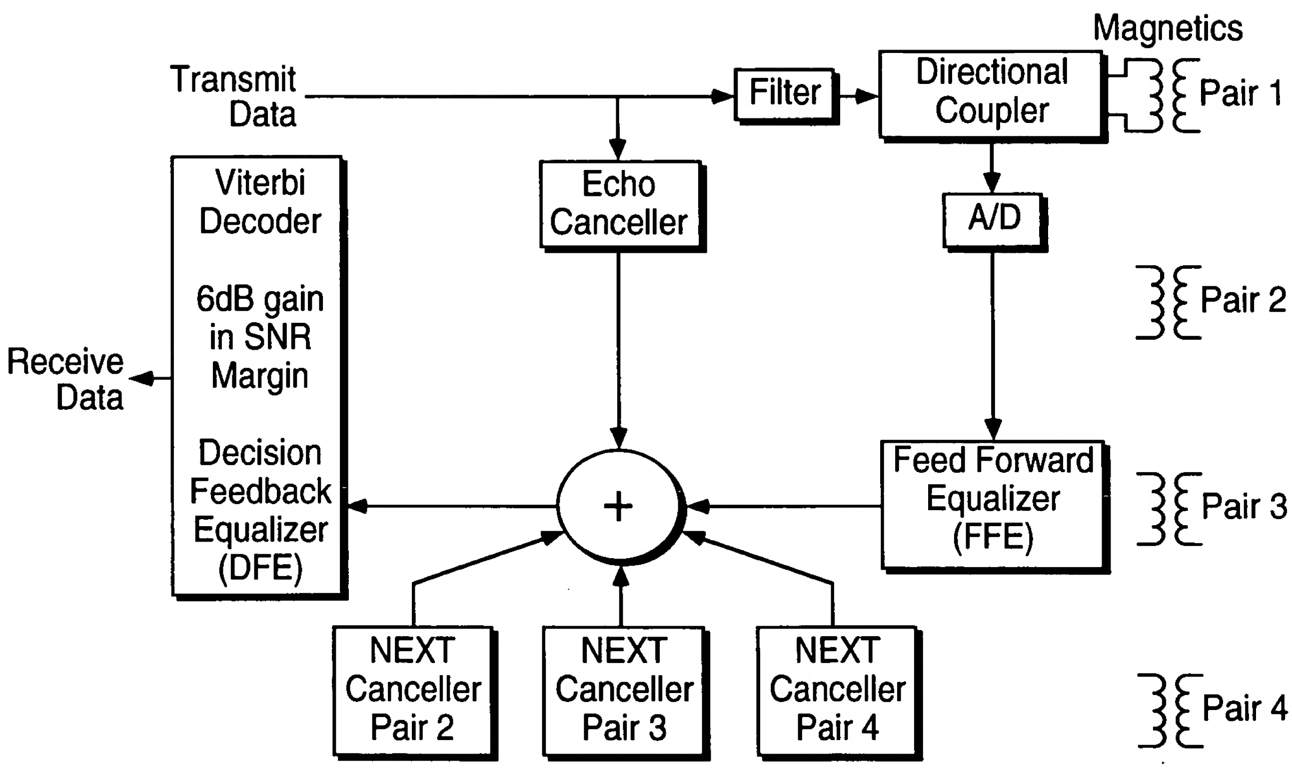


FIG. 8

Typical Parallel Channels for ECHO, NEXT and FEXT Cancellations

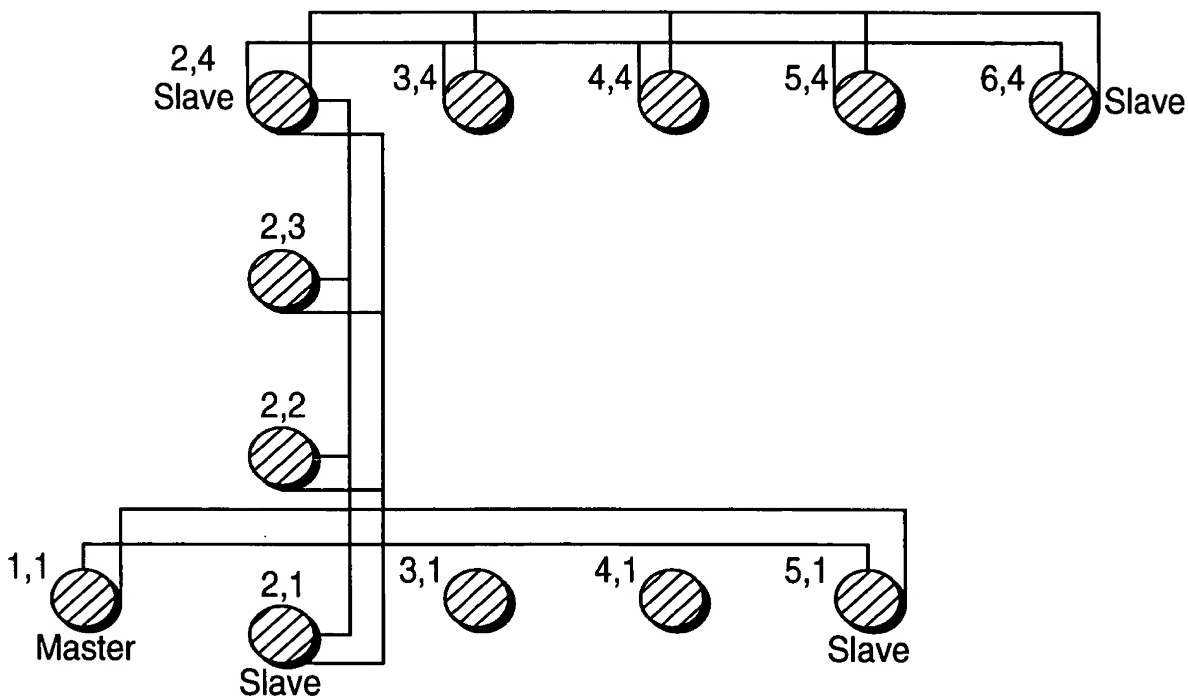
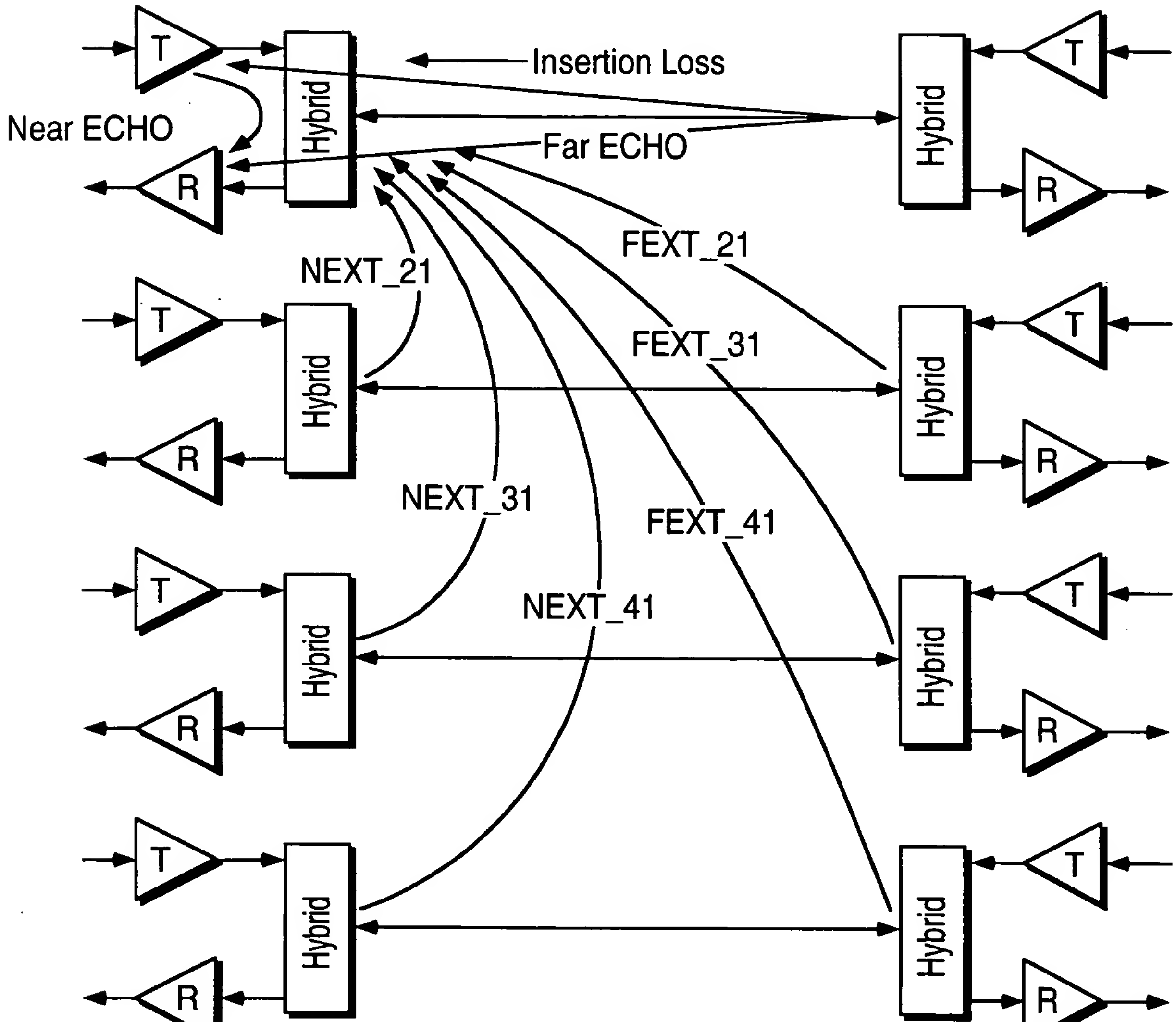


FIG. 9

UniNet Hierarchical Synchronization



(using 4 wire pairs)

FIG. 10

Gigabit Ethernet over 4 pairs of UTP cables

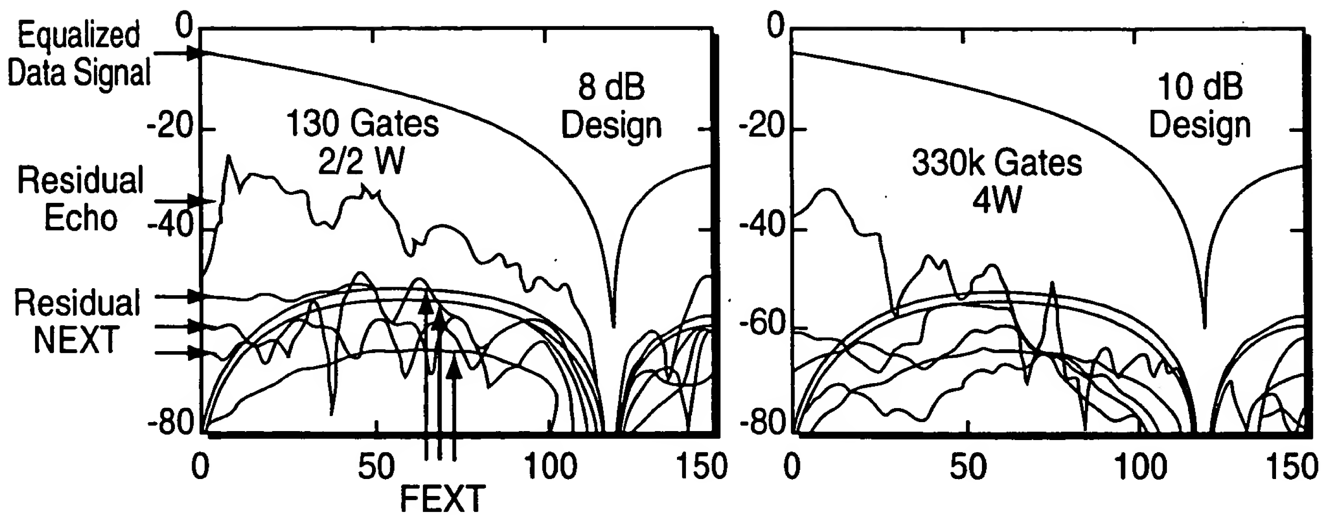


FIG. 11A

	3 dB Design	10 dB Design
Margin without FEXT	3.5 dB	10.7 dB
Margin with FEXT	2.5 dB	6.7 dB
Margin with FEXT + 3	1.8 dB	4.9 dB

FIG. 11B

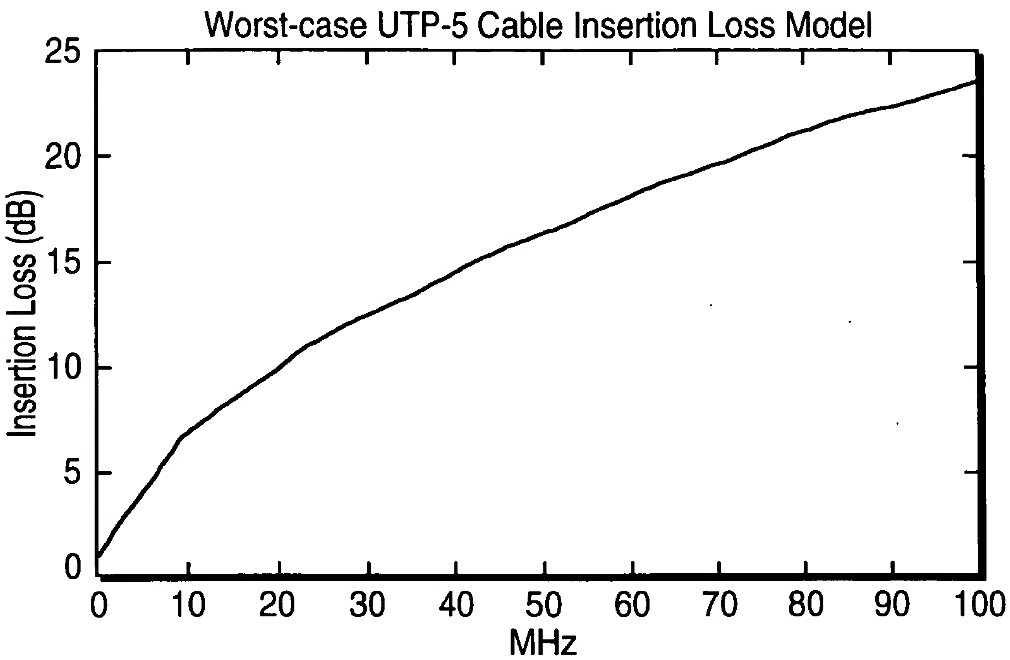


FIG. 12A

Worst-case Insertion Loss of 100m, cat-5 Cable

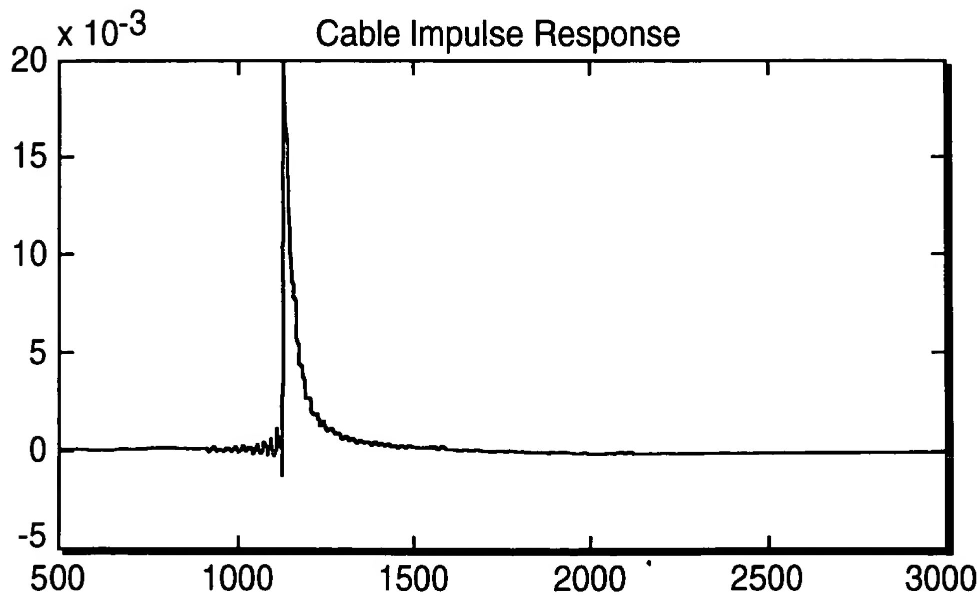


FIG. 12B

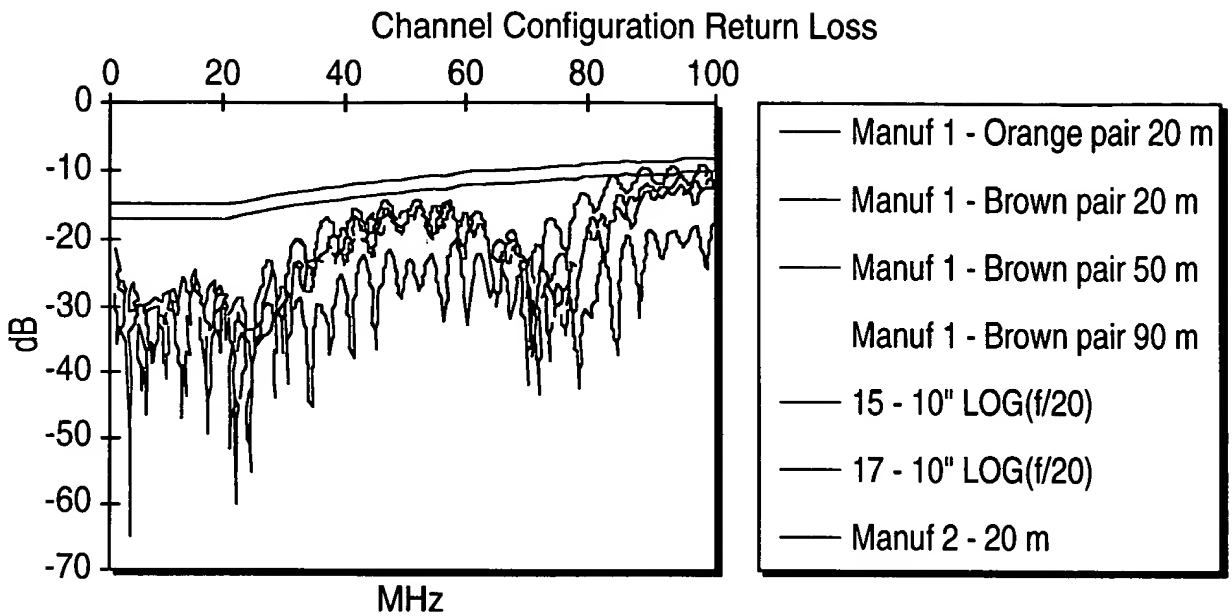


FIG. 13A

Overall Return Loss of Different Cable Channel

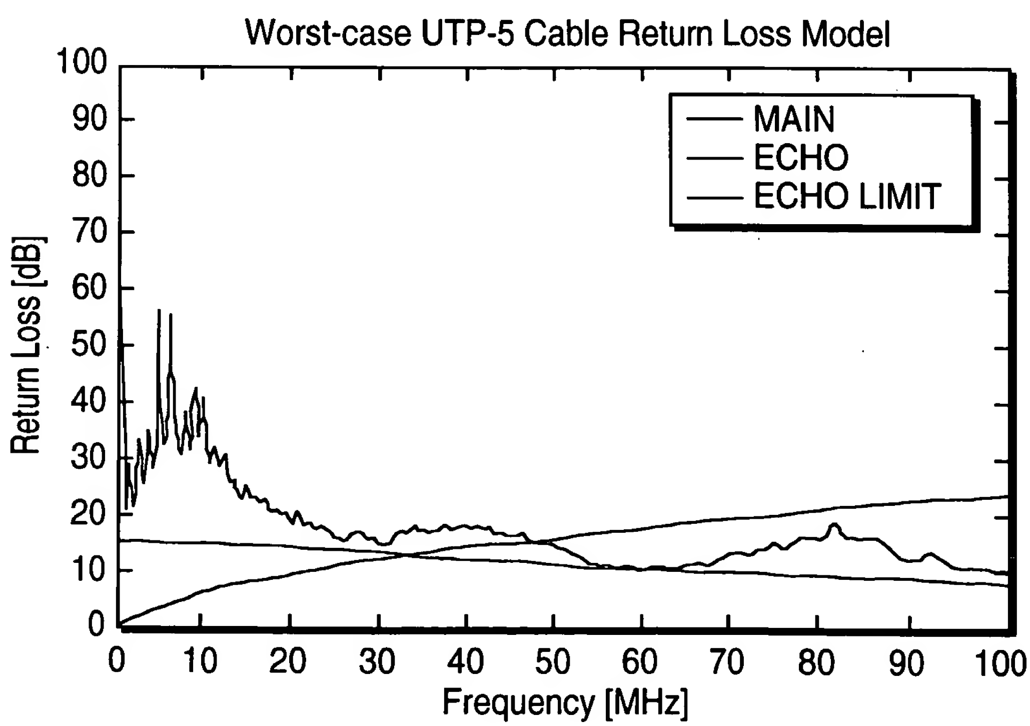


FIG. 13B

Worst Case Return Loss Relative to Main Signal

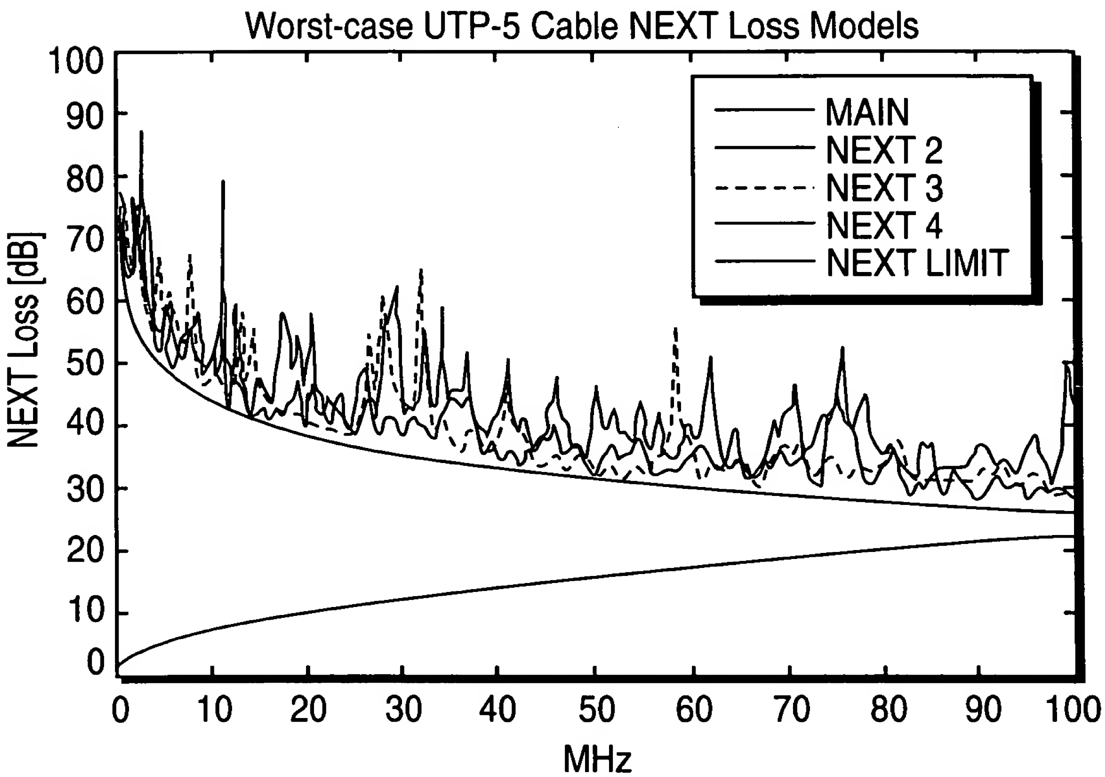


FIG. 14

NEXT loss between pairs of cat-5 cables

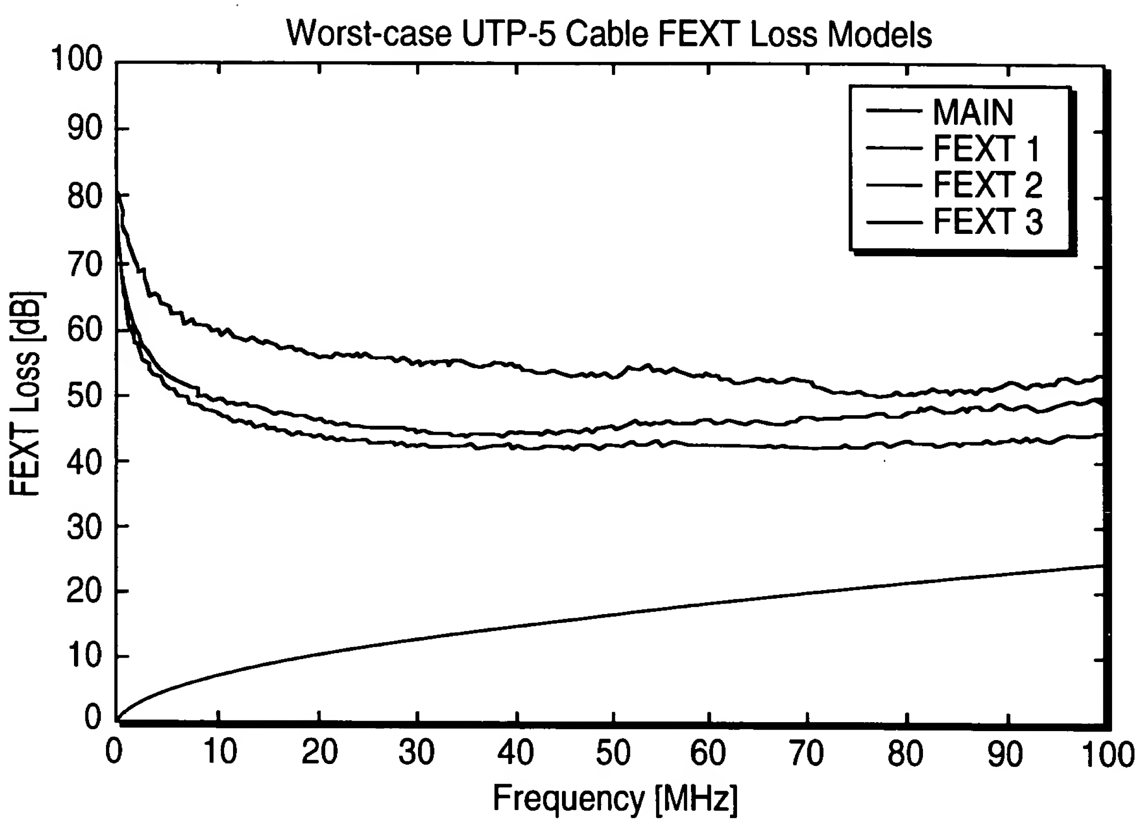


FIG. 15

FEXT Loss Characteristics

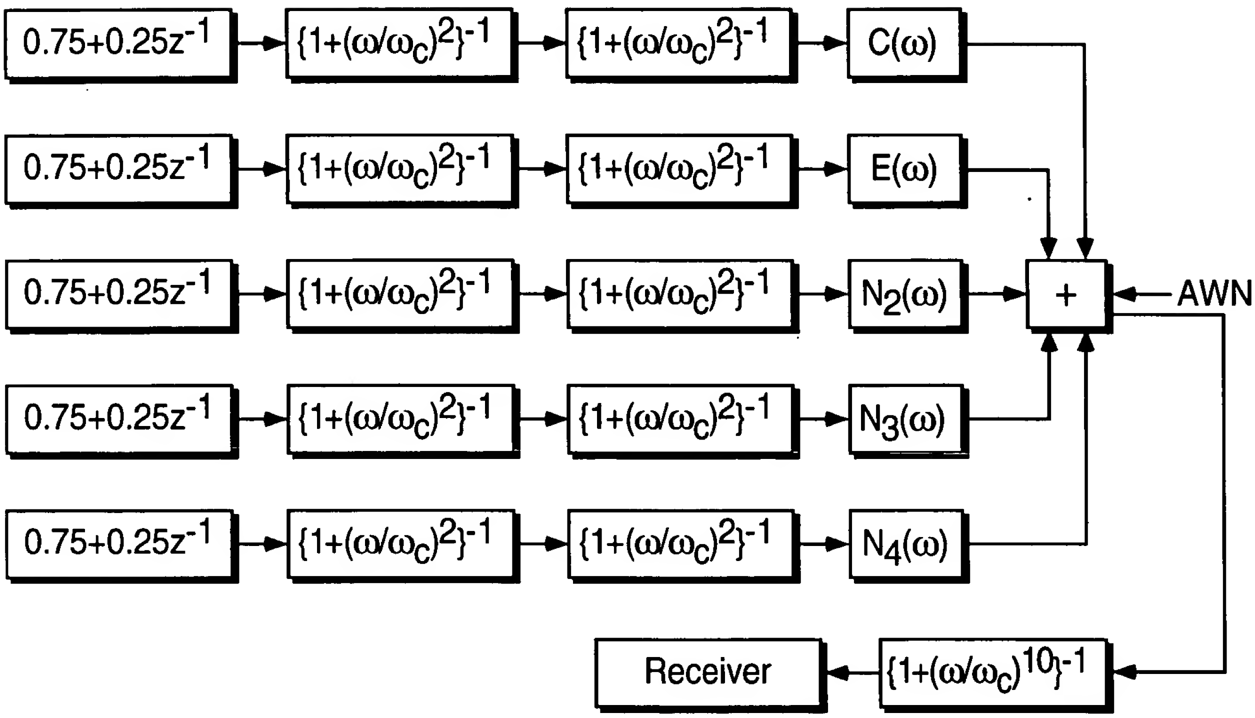


FIG. 16

System Modeling

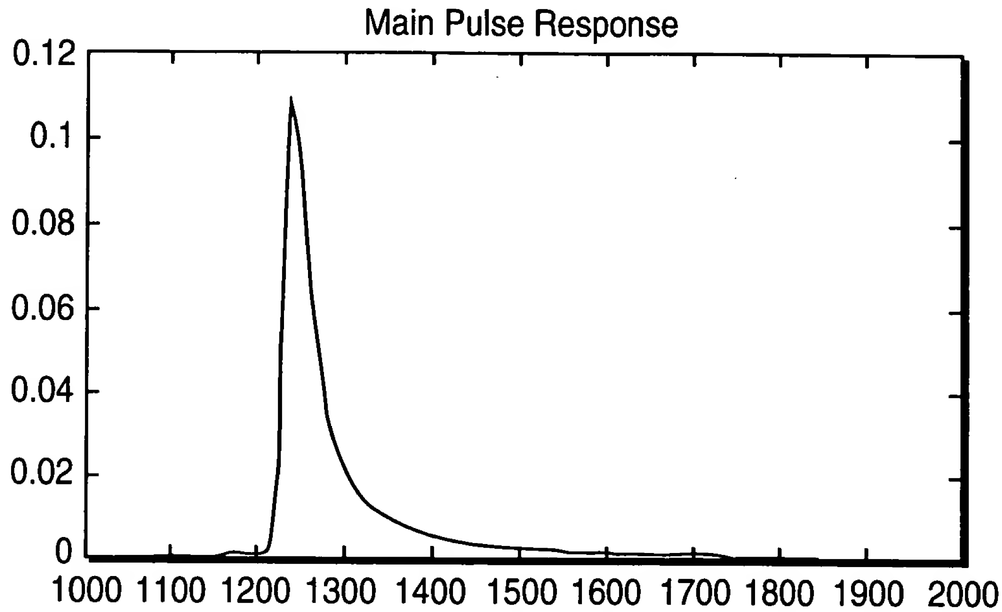


FIG. 17

Received (desired) pulse response

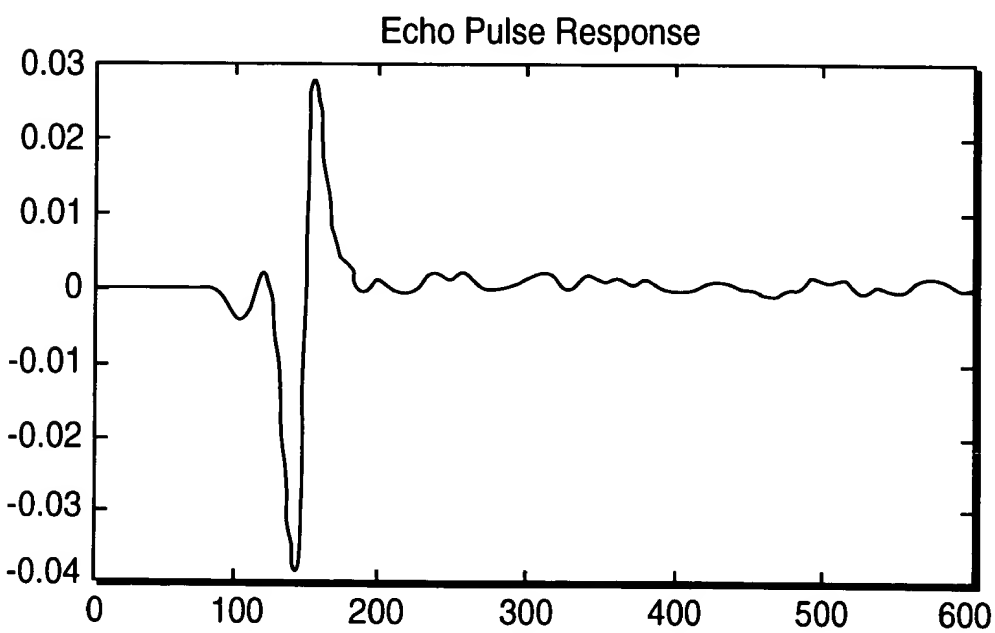


FIG. 18

Echo Pulse Response

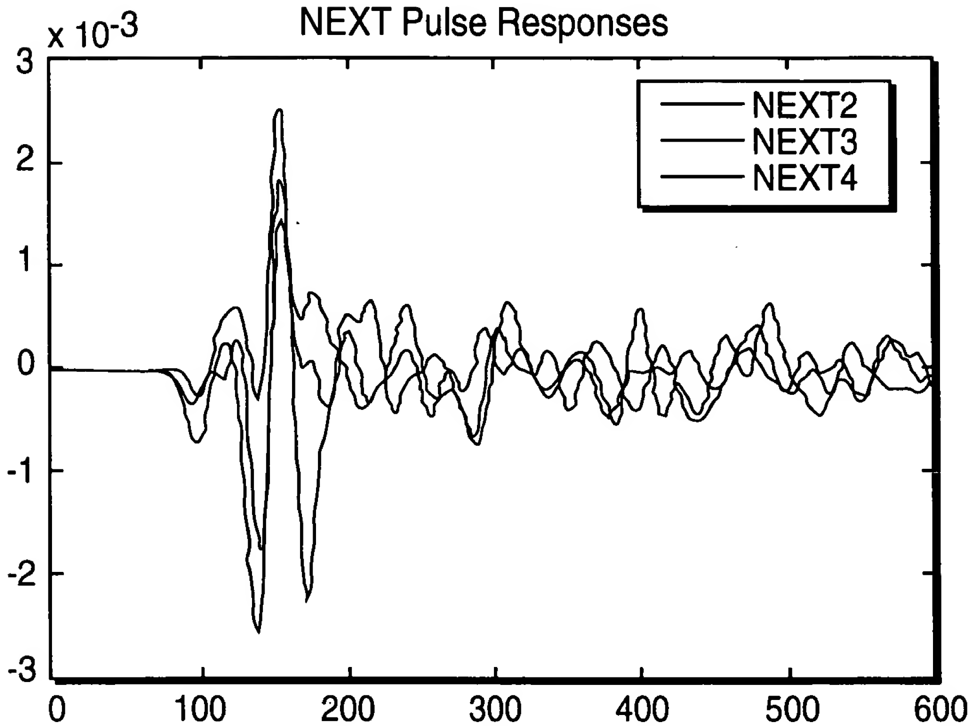


FIG. 19A
NEXT Pulse Responses

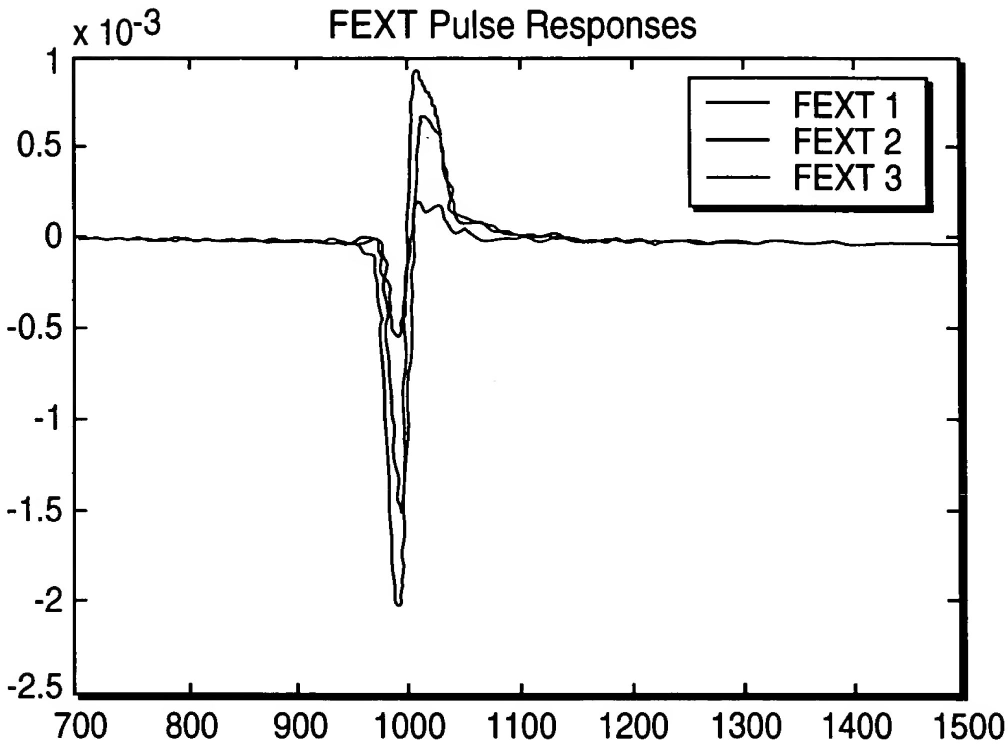


FIG. 19B
NEXT Pulse Responses

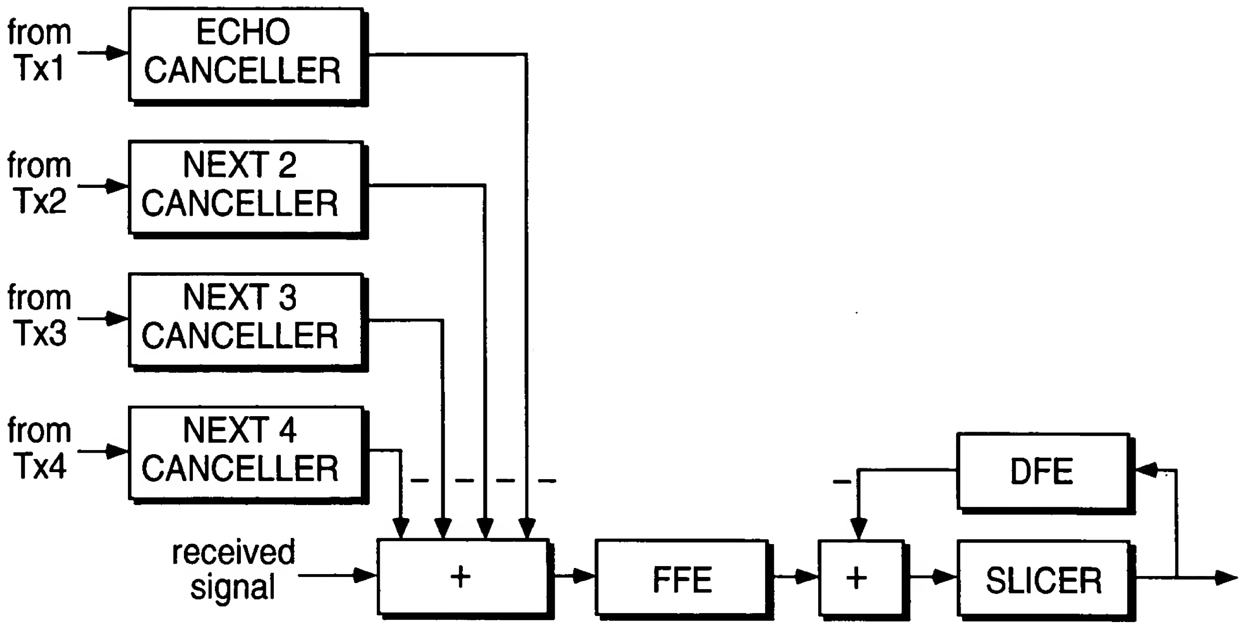


FIG. 20A

Receiver Structure Using Interference Cancellers Prior to Equalizers

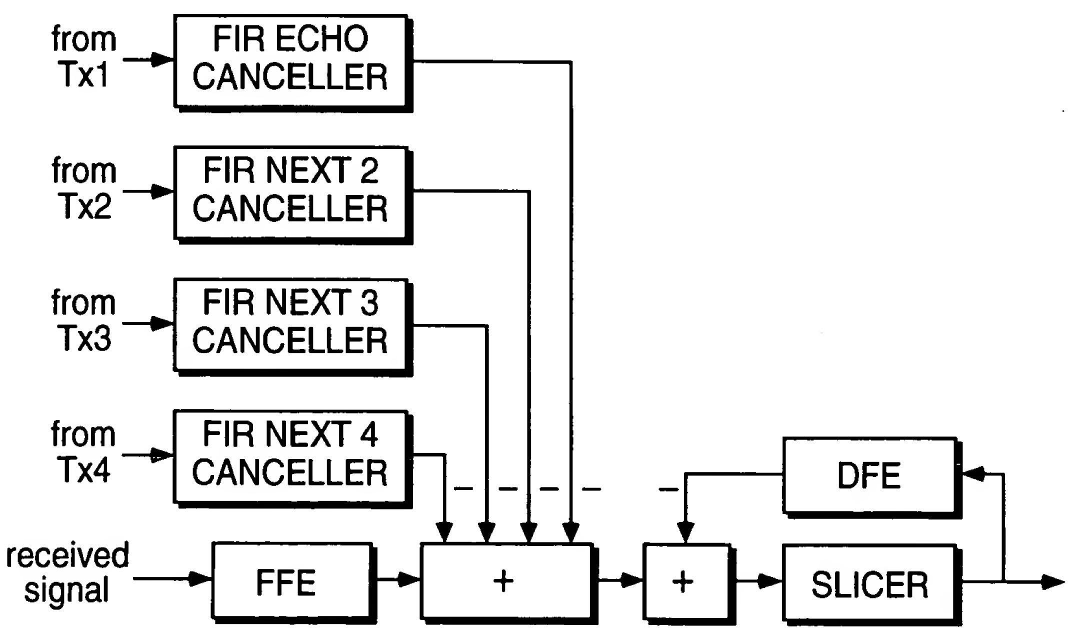


FIG. 20B

Receiver Using Interference Cancellers After FFE

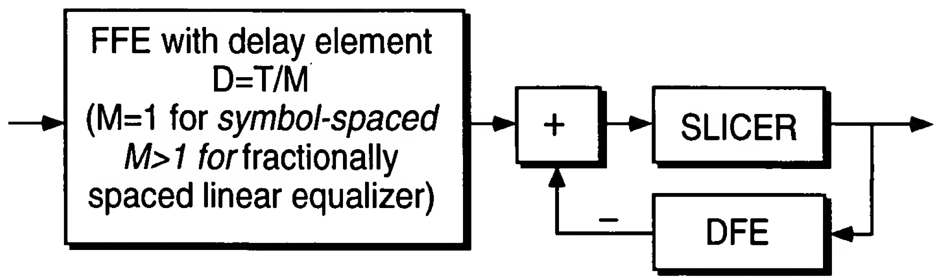


FIG. 20C

Receiver using cascaded FSLE/DFE for both interference suppression and equalization

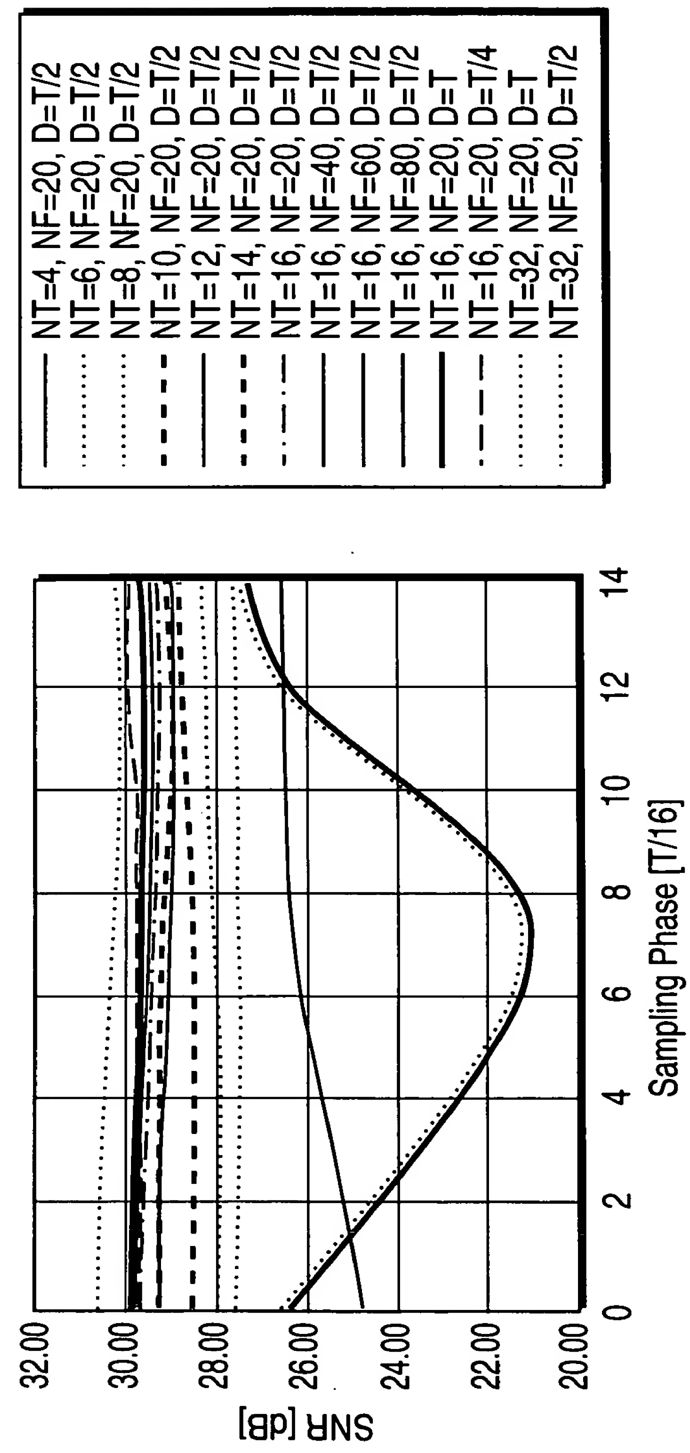


FIG. 21

SNR versus Sampling Phase of different FFE/DFE configurations

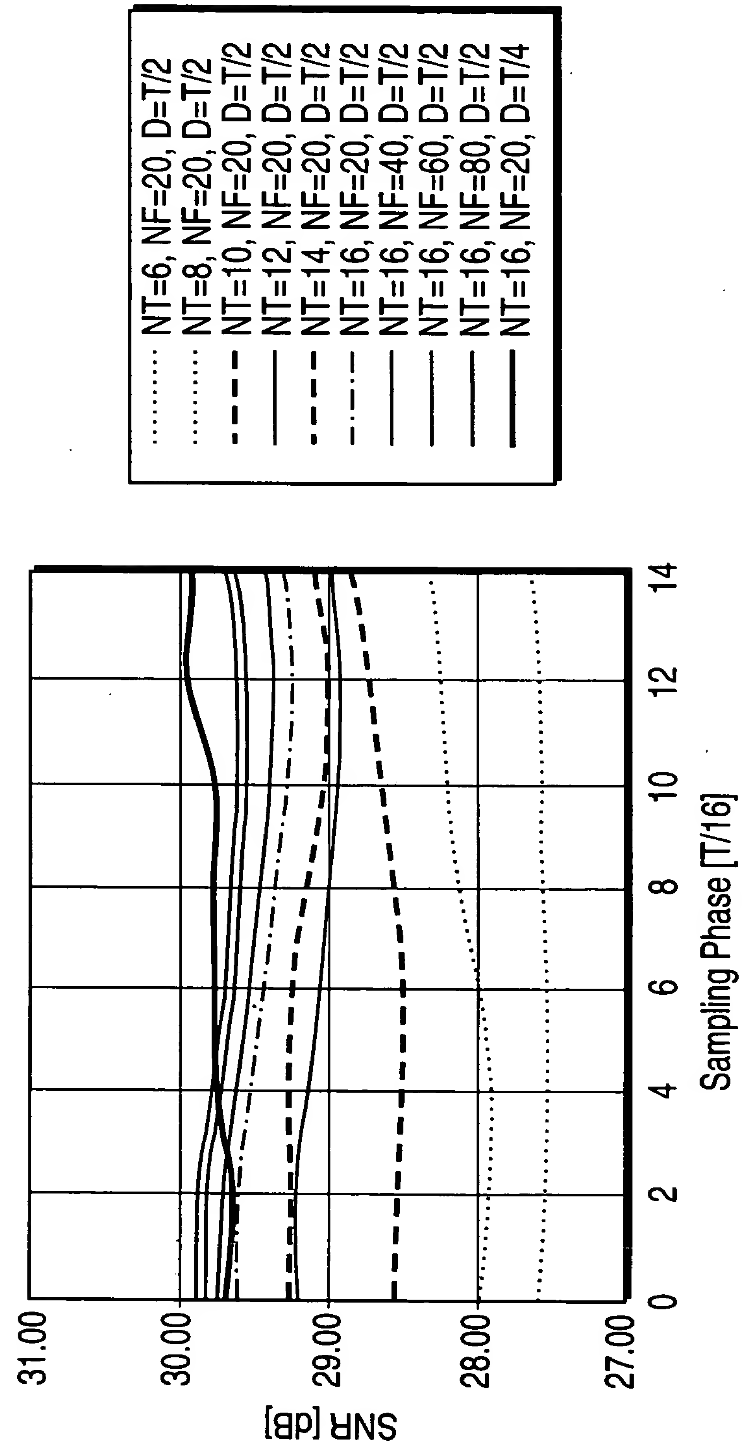


FIG. 22

SNR versus Sampling Phase for various FSLE/DFE configurations

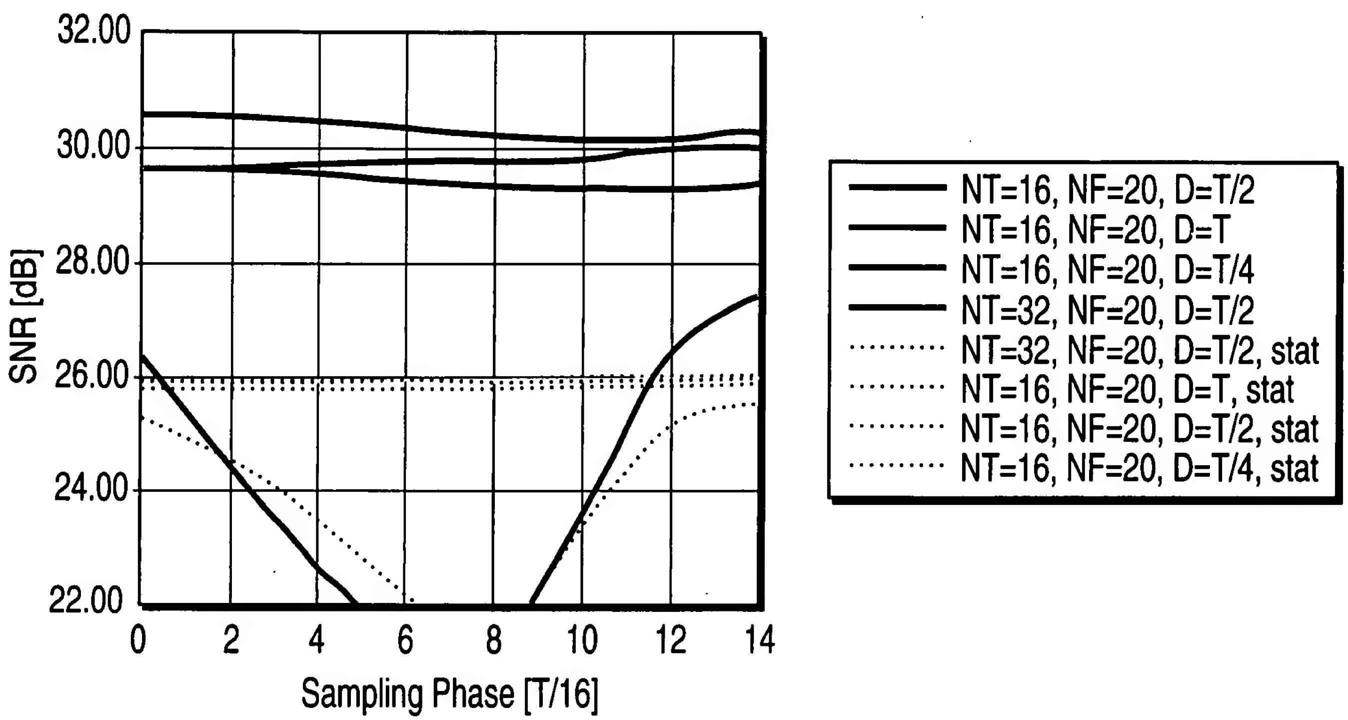


FIG. 23

SNR vs Sampling Phase

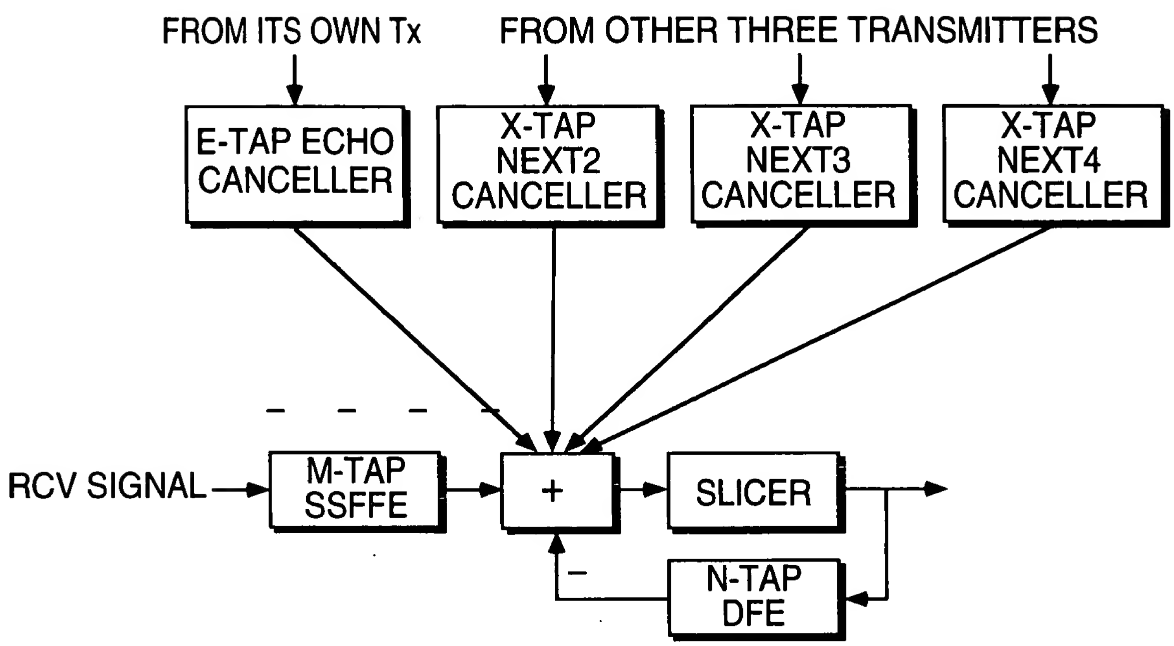


FIG. 24

Currently Proposed Structure

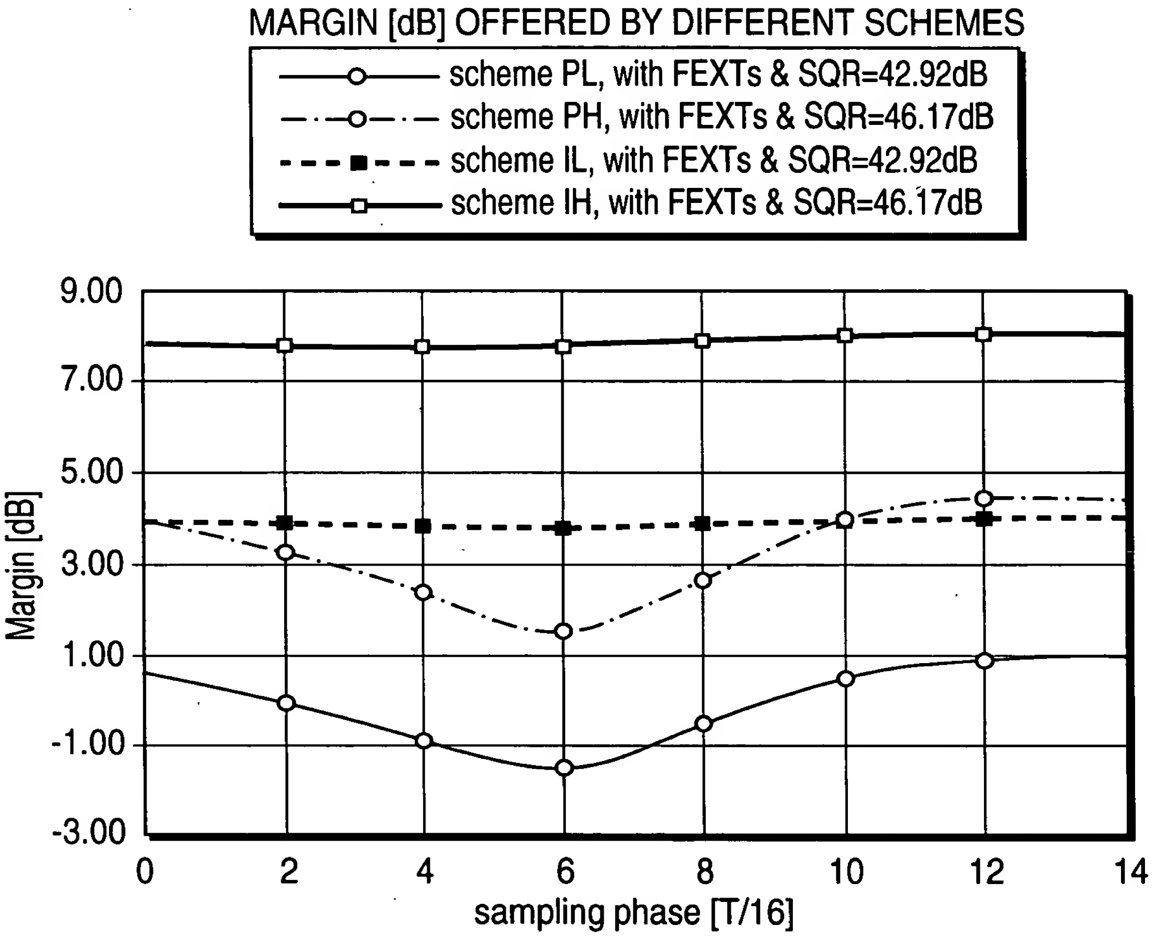


FIG. 25

Margin Offered by Different Schemes

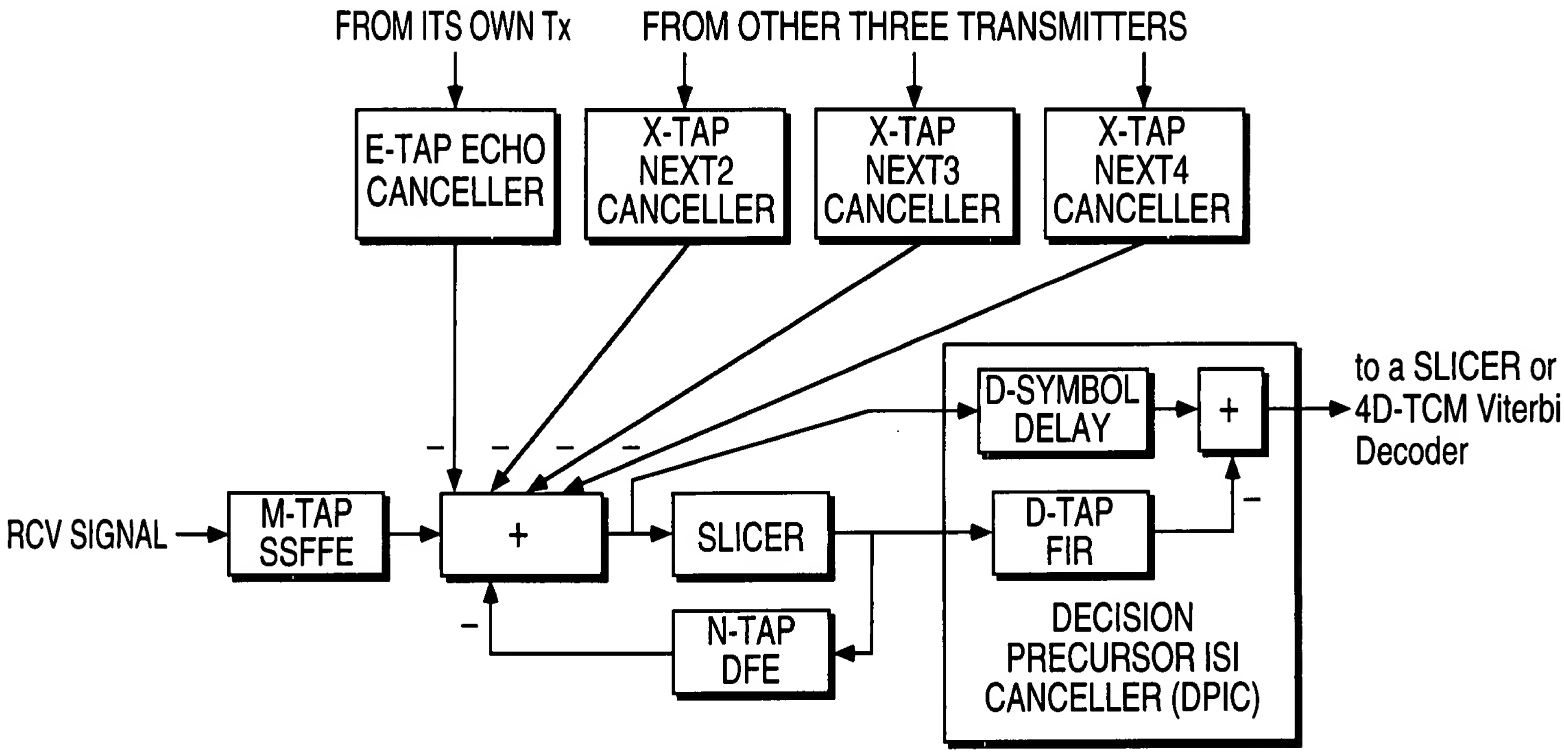


FIG. 26

Improved-Performance Receiver Structure

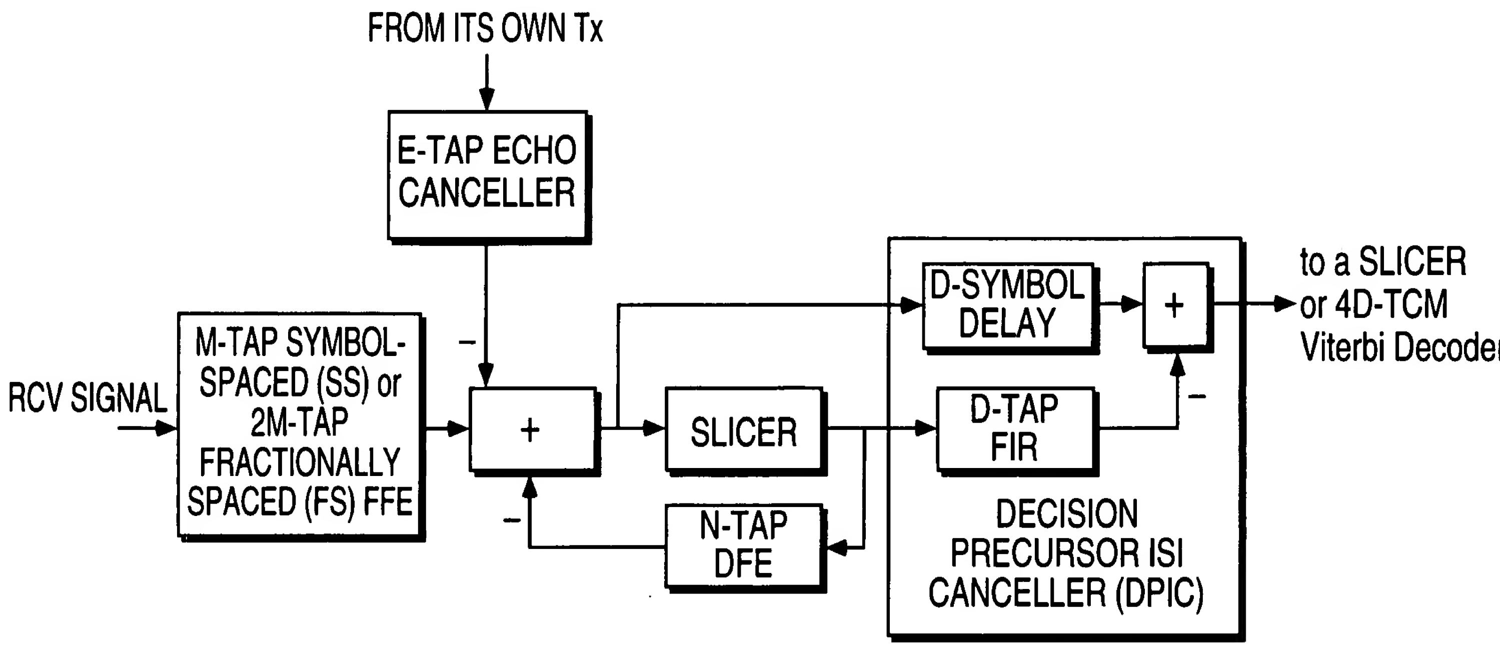


FIG. 27

Receiver Structure using DPIC without NEXT cancellers

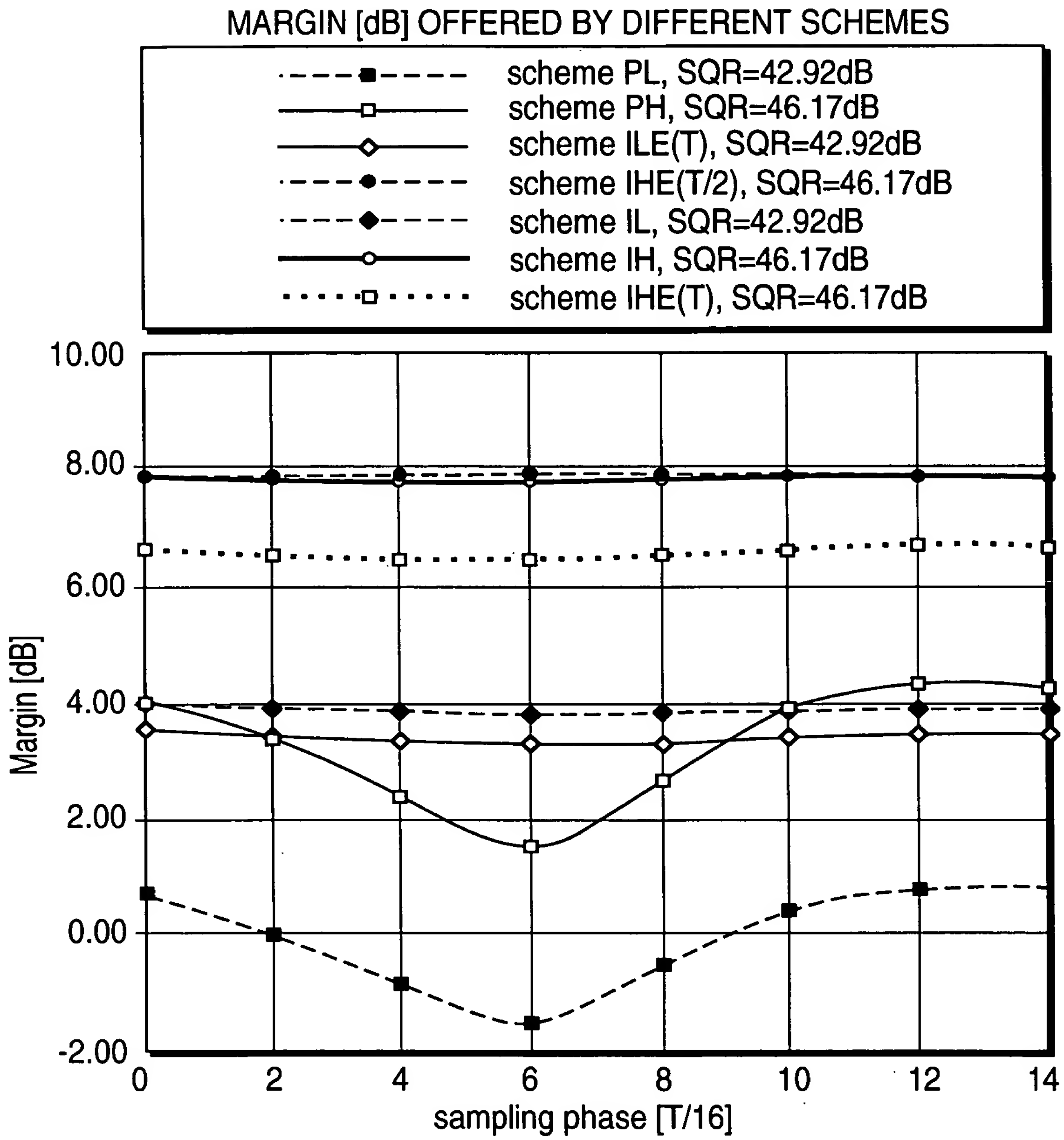


FIG. 28

Margin Offered by Various Schemes

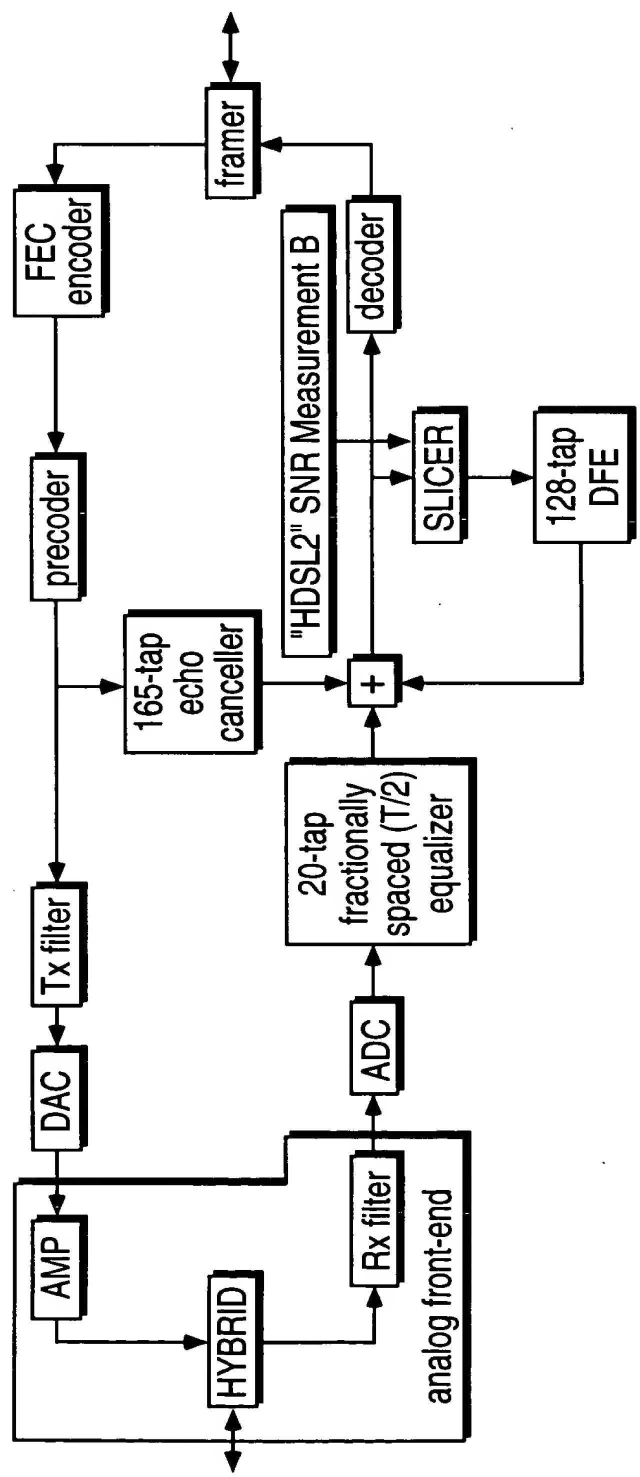


FIG. 29

Existing SHDSL Transceiver Structure

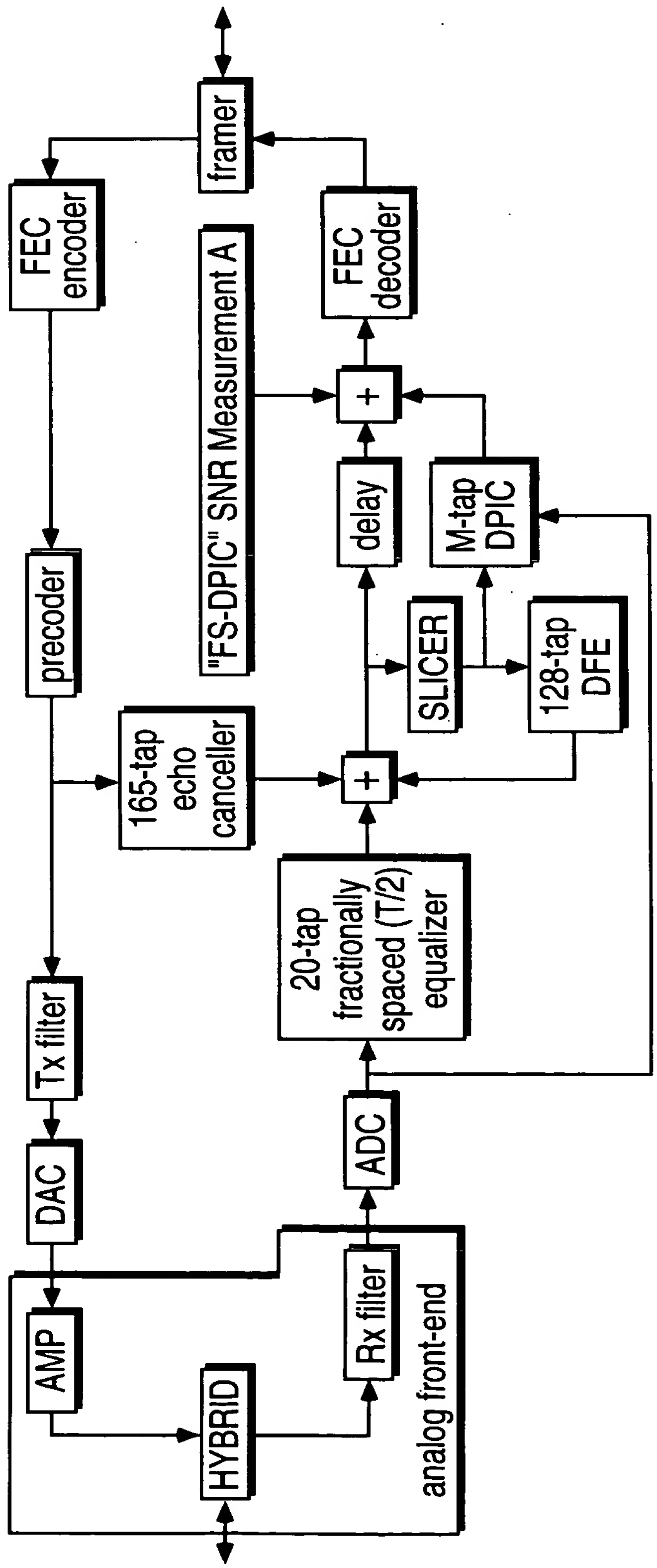


FIG. 30
Proposed Transceiver Structure using DPIC

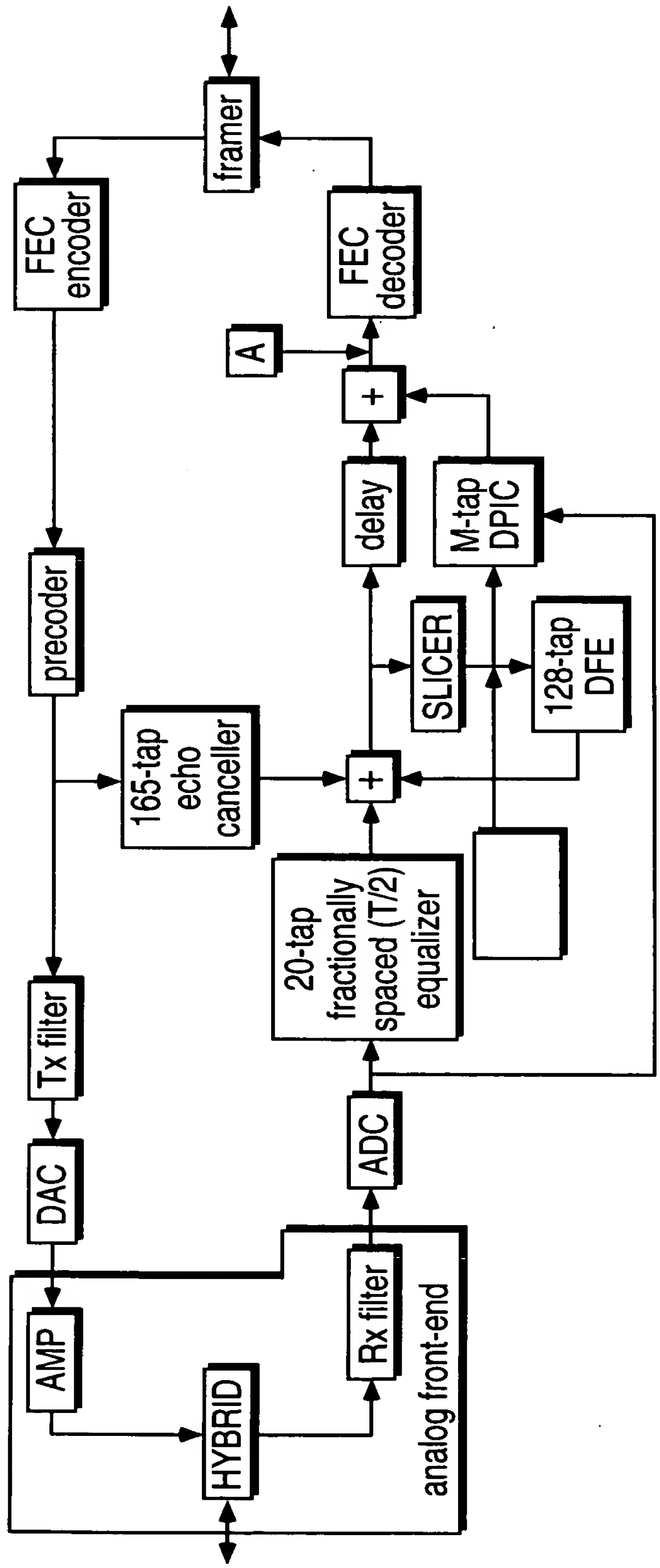


FIG. 31

SNR Measurement Points (A,B) (Proposed Transceiver Structure using DPIC)

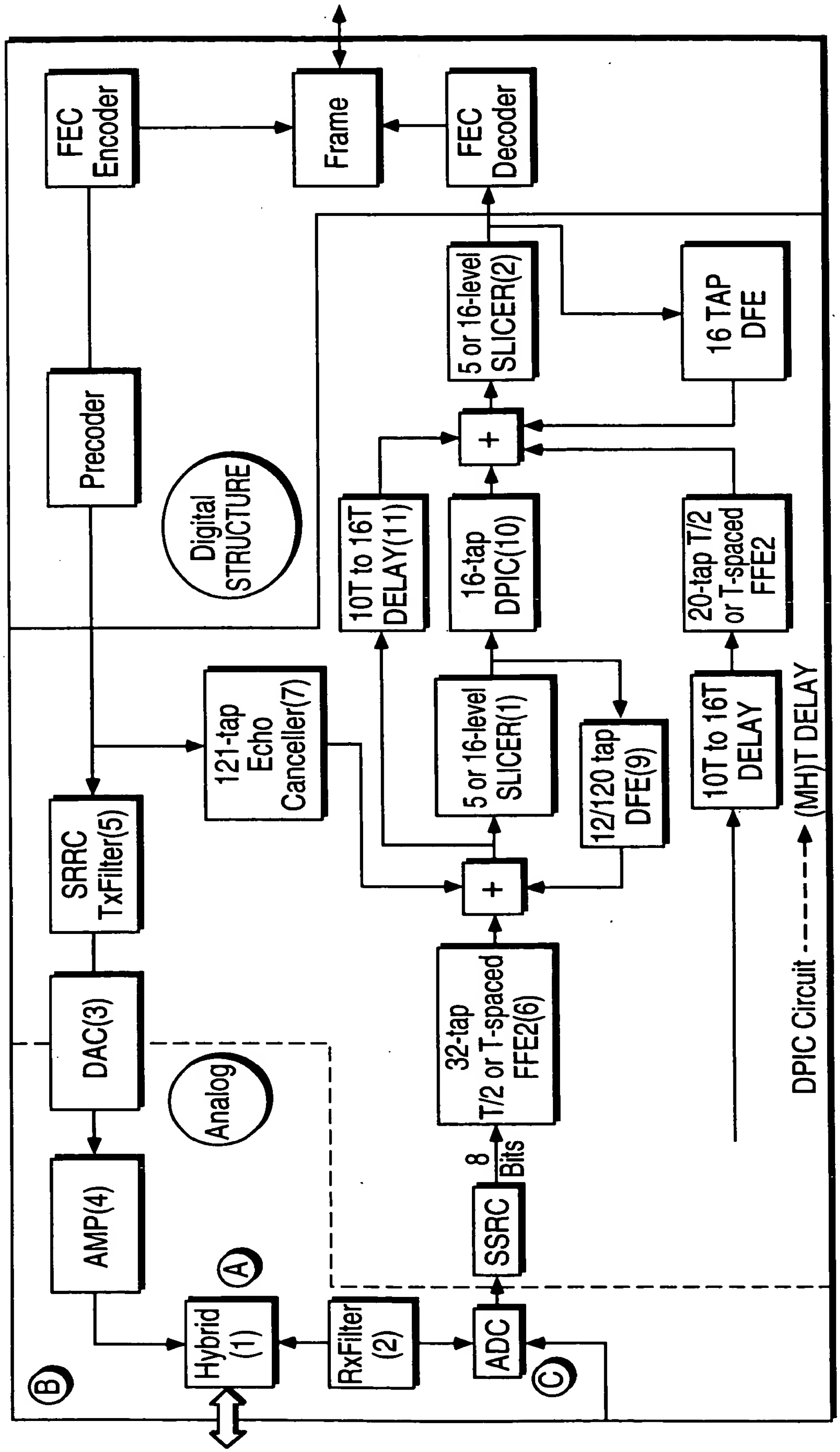


FIG. 32

HDSL2 Front-End (Converter & Sampler & Equalizers)

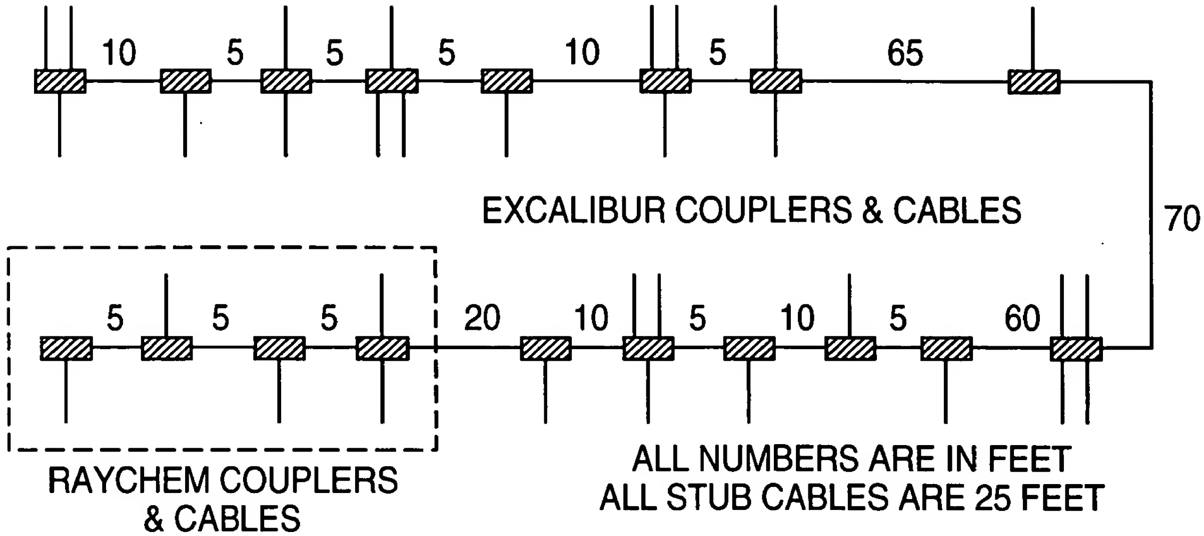


FIG. 33A
SAE Developed De Long Network

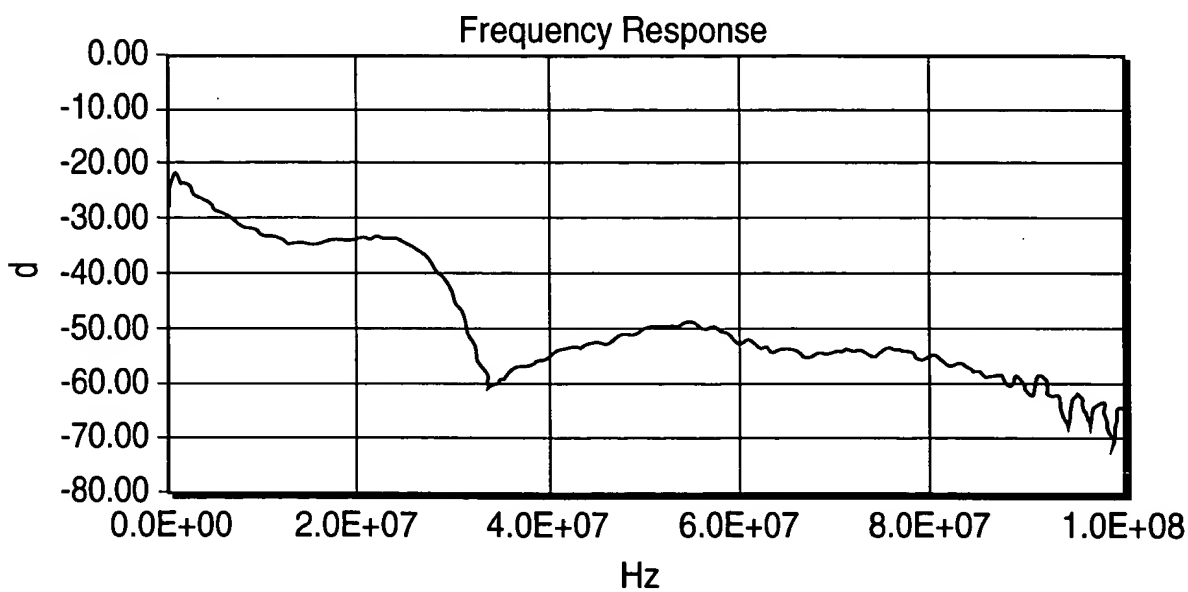


FIG. 33B
SAE Developed De Long Network Impulse Response

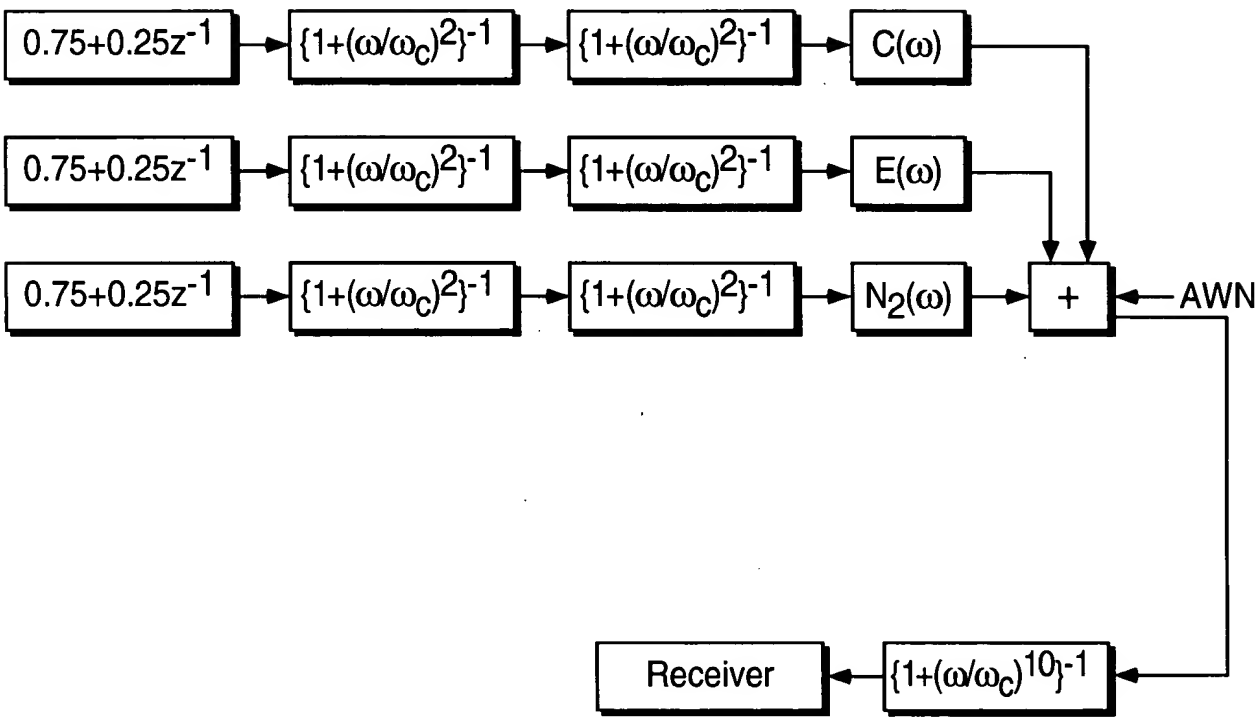
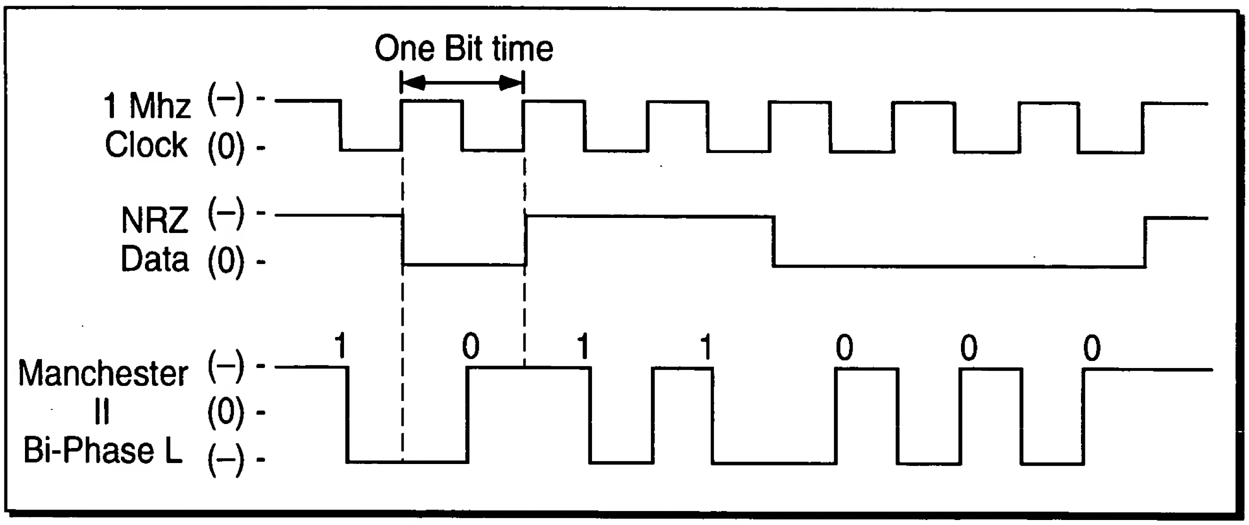


FIG. 34

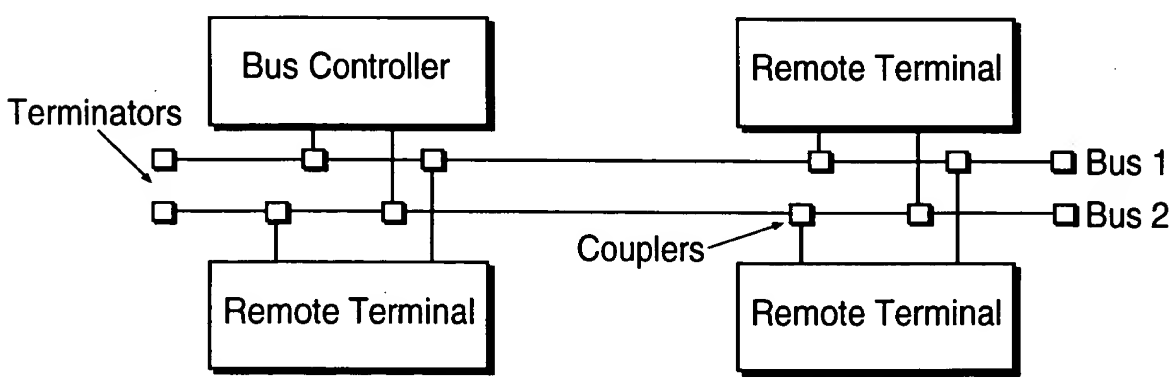
Next Generation 1553 System Modeling

FIG. 35

Current 1553 Architecture and Data Coding Scheme



Data Coding Scheme of Current 1553 Data Transmissions



Example of Current 1553 Bus Cabling Architecture (Redundant)

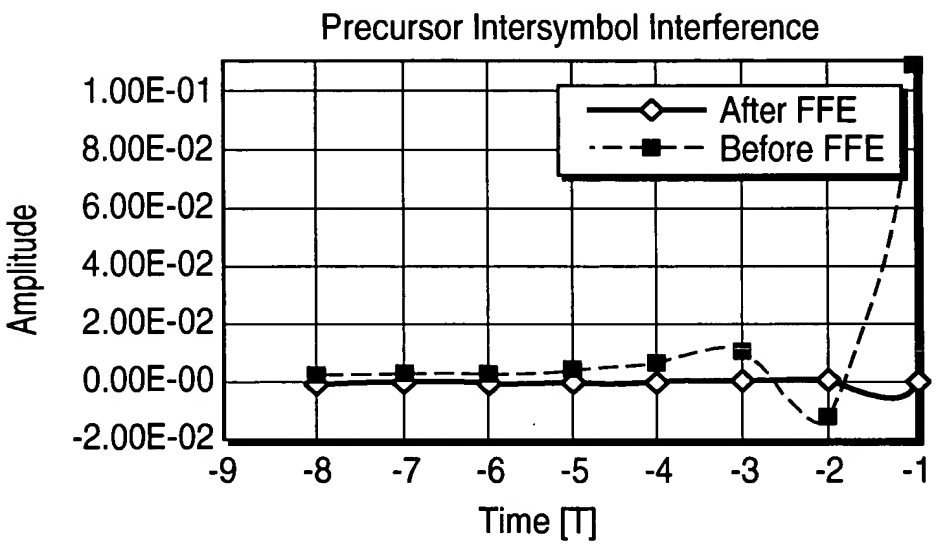
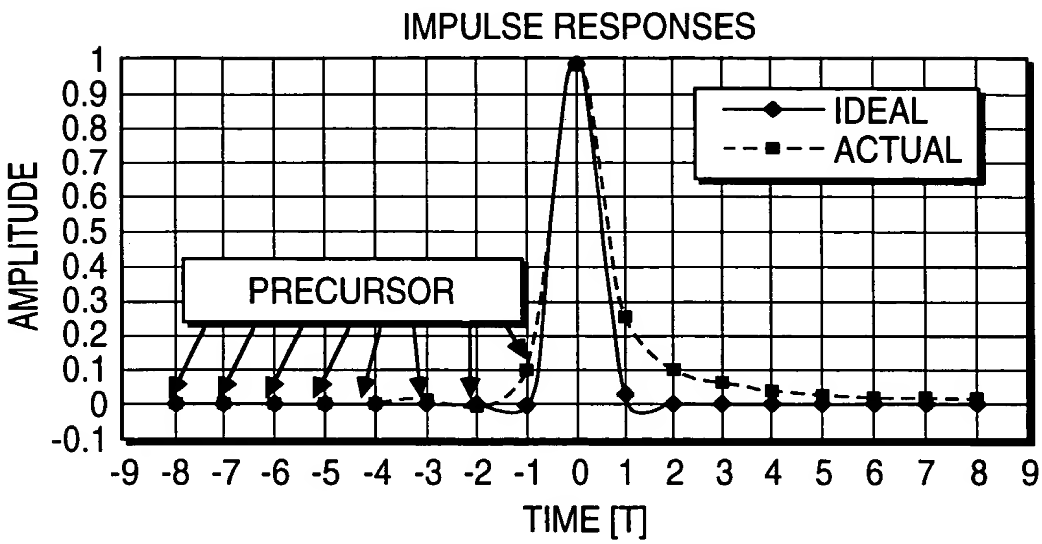


FIG. 36

Before and After Fractional Space Equalizer for Precursor ISI



100Mb/s USING PAM 8 over a 100m-cable

FIG. 37

Intersymbol Interference (ISI) at High Transmission Rate Over MIL-C17 Cable

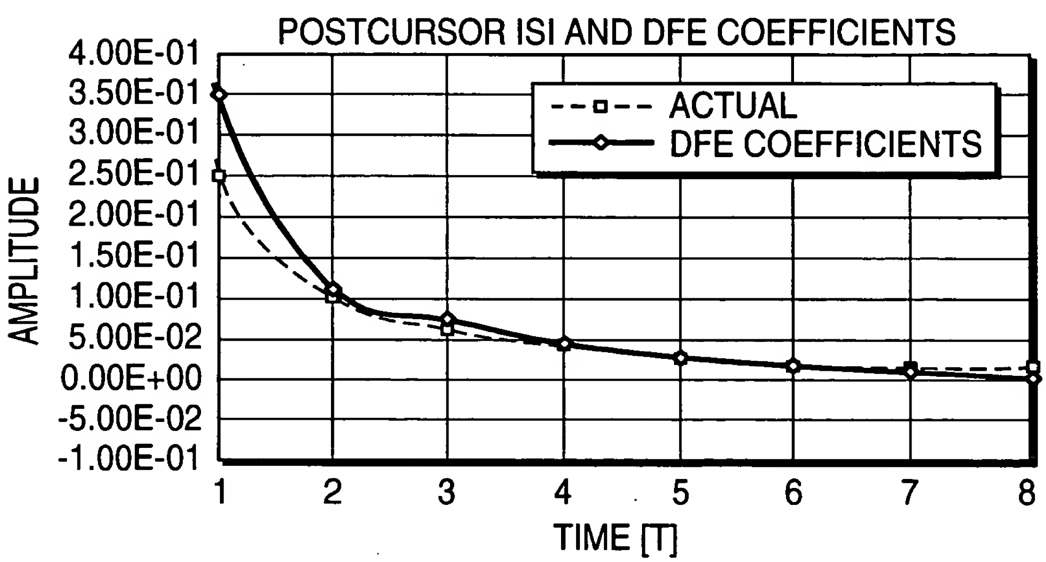


FIG. 38

Decision Feedback Equalization to Remove Postcursor ISI

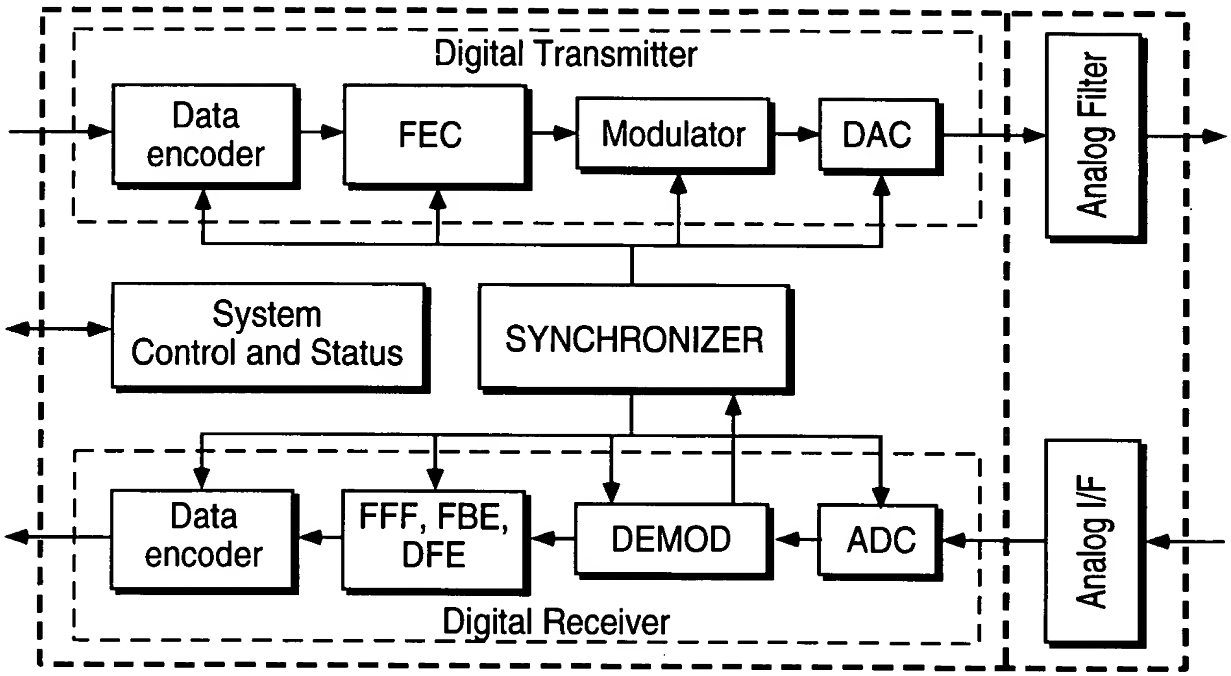


FIG. 39A

Proposed High Level 1553+ Transceiver Structure High Level

Title: "Channel Equalization System And Method"
Inventors: Francois Trans & Tho Le-Ngoc
Atty. Docket No.: 20870-06001; Case 6001 US
Application No.: Not Yet Known

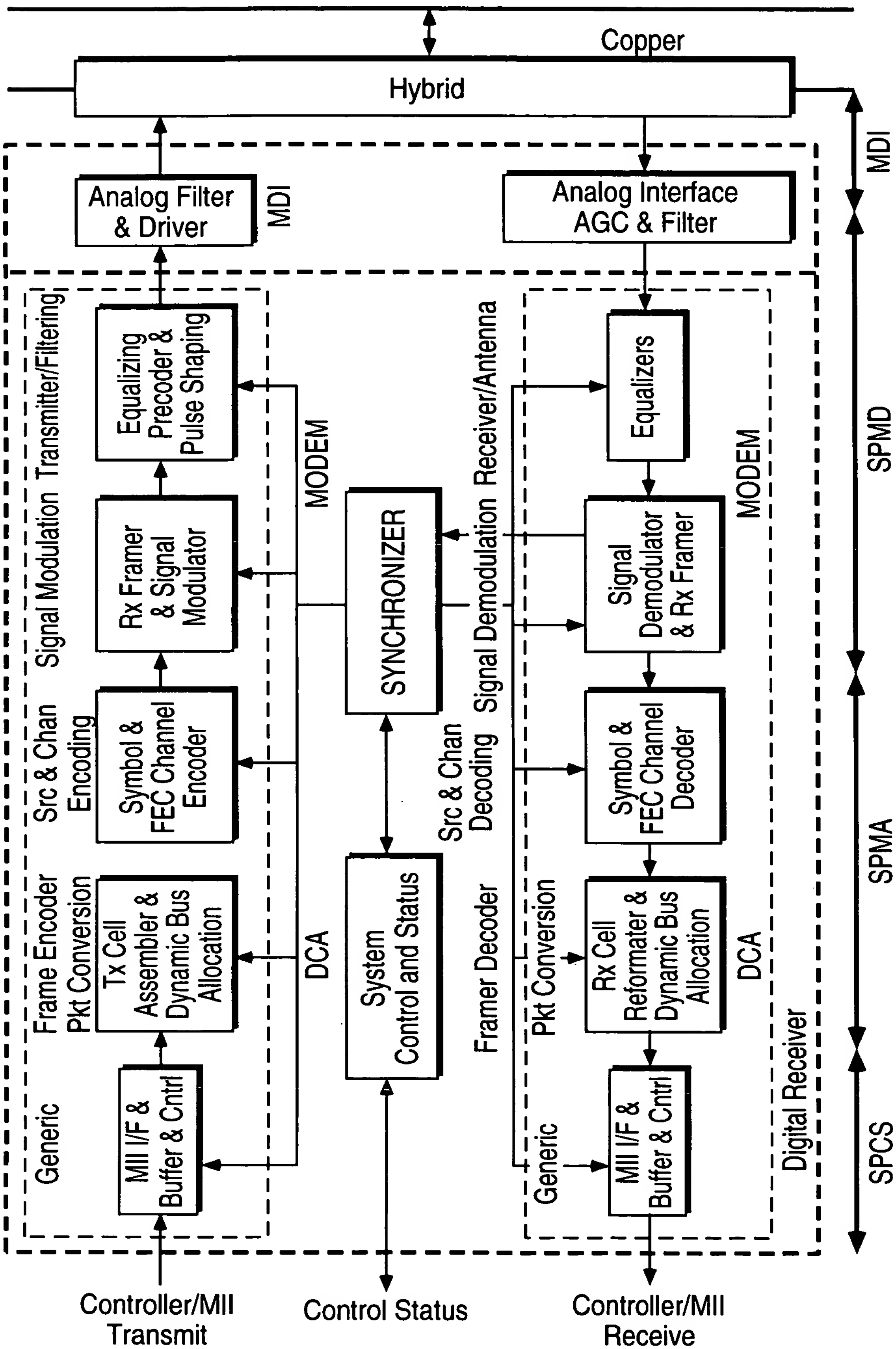


FIG. 39B

Proposed Medium Level 100Mb/s1553+ Transceiver Structure High Level

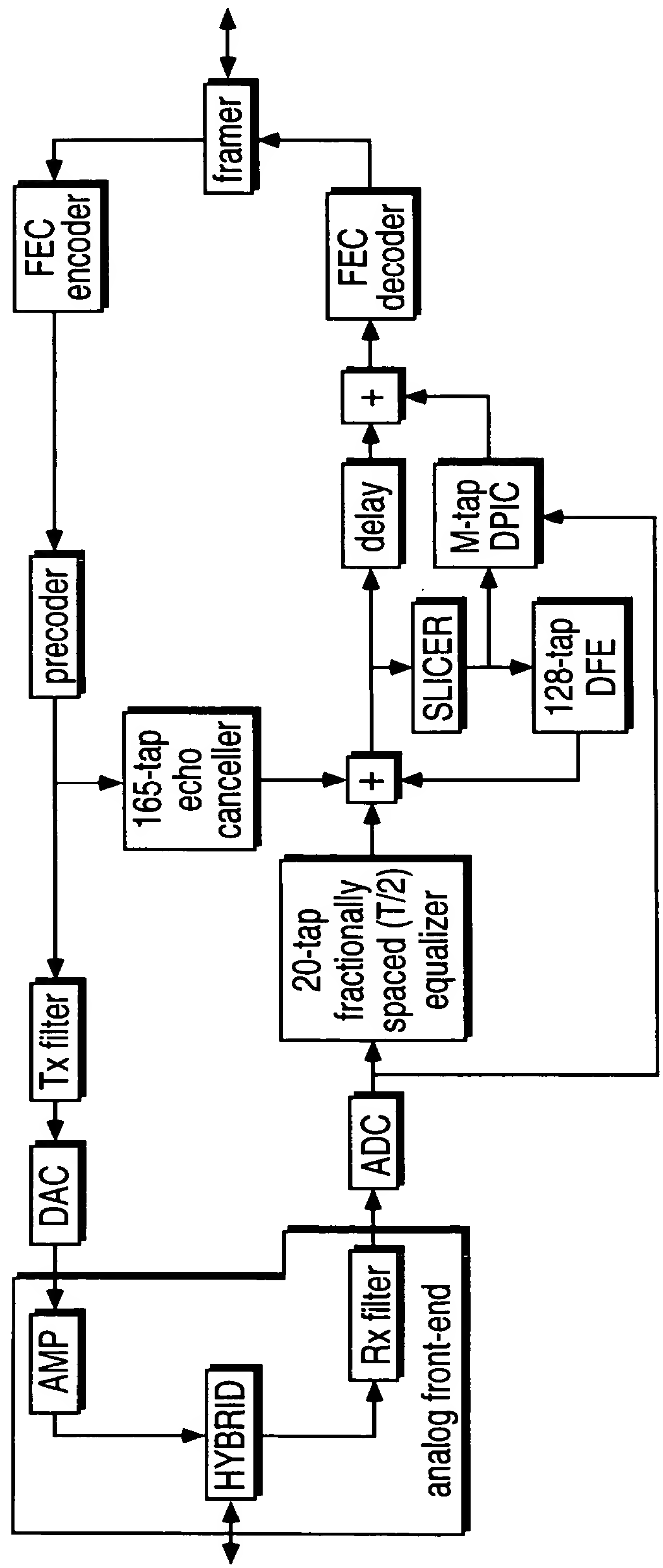


FIG. 39C

Proposed Detailed 100Mb/s 1553+ Transceiver Structure using DPIC

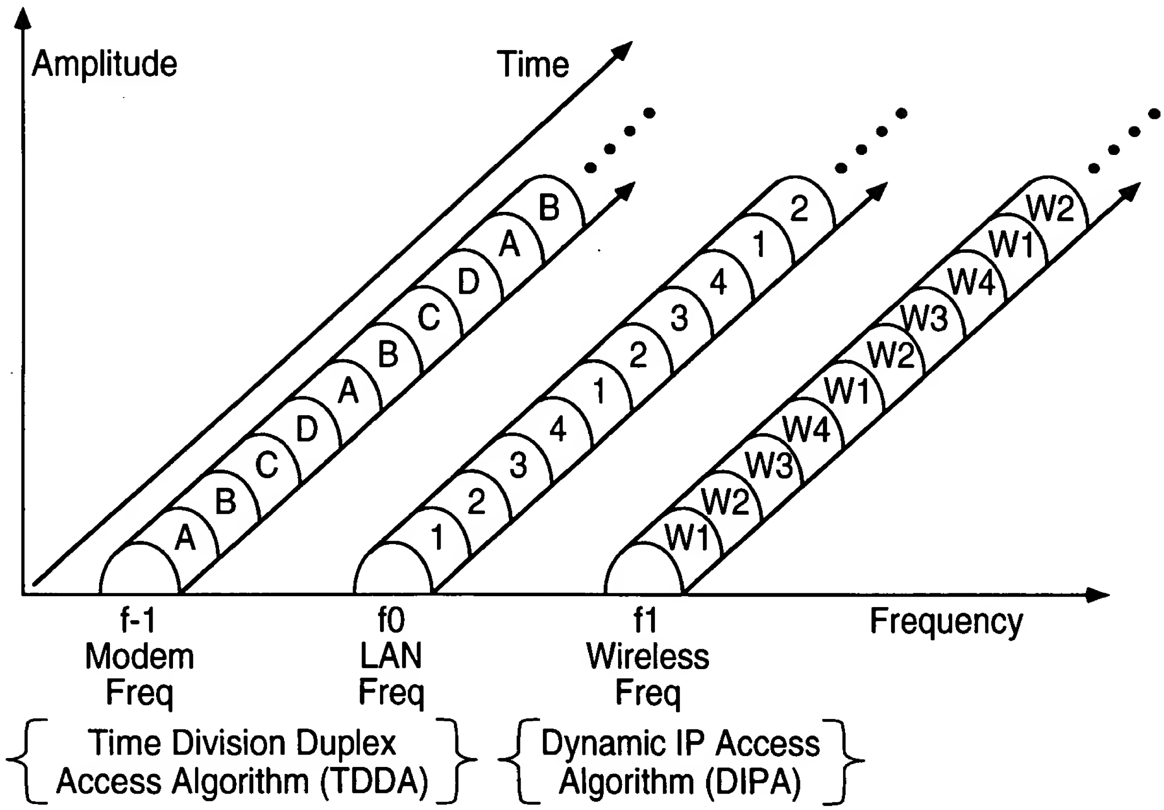


FIG. 40

Channelization/Timer Division Multiplex Access (TDMA/TDD)

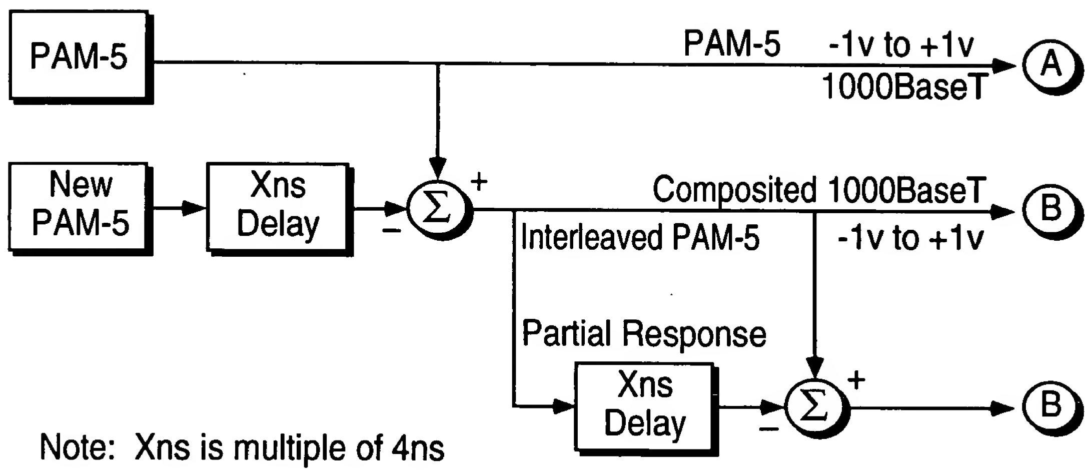


FIG. 41
Com2000™ PAM-5 Partial Response Signaling Overview

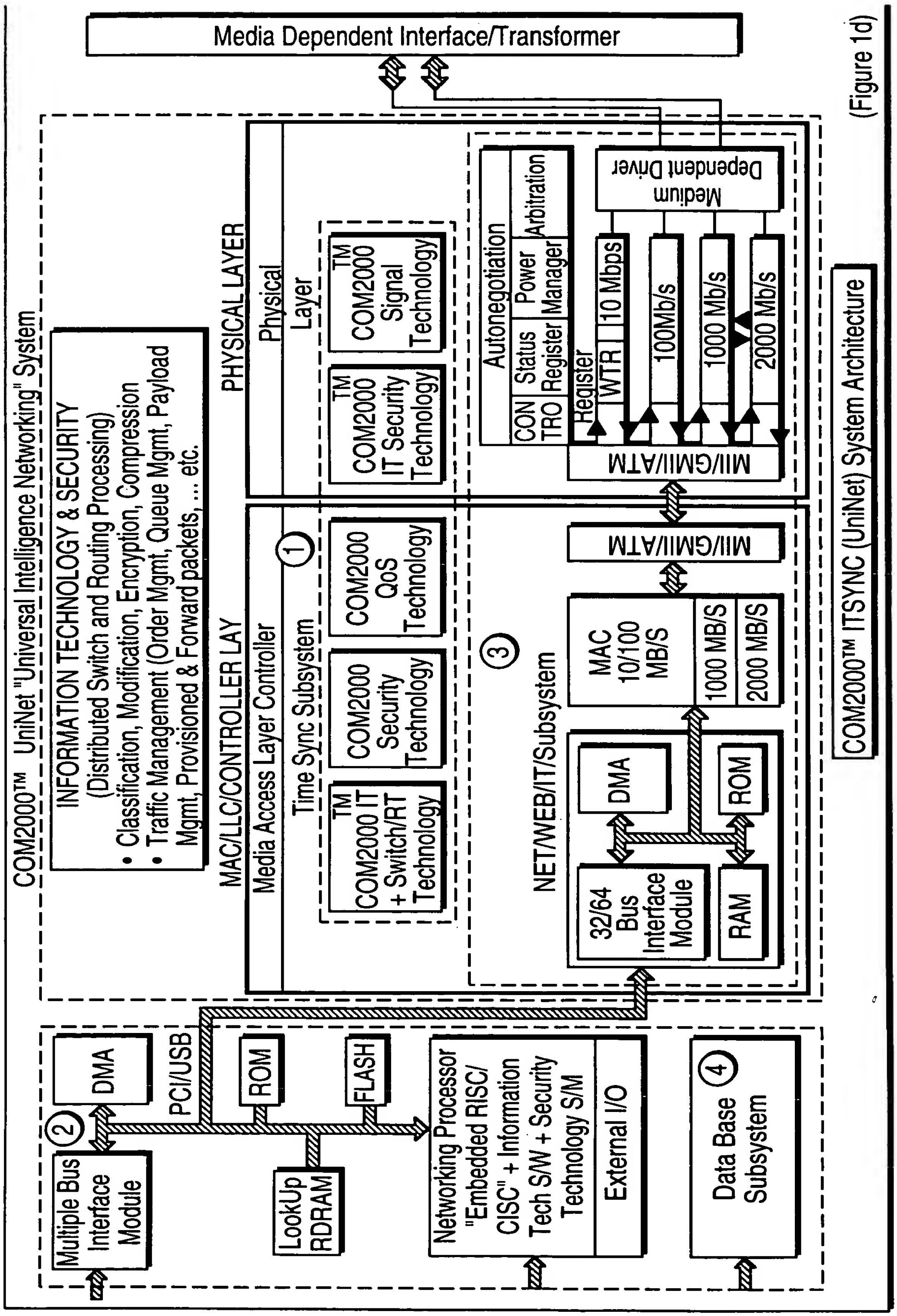


FIG. 42
UniNet Internet Communication Processor

Title: "Channel Equalization System And Method"
ntors: Francois Trans & Tho Le-Ngoc
Docket No.: 20870-06001; Case 6001 US
plication No.: Not Yet Known
Sheet 45 of 97

FIG. 43
Com2000™ Clock Transfer Subsystem Block Diagram

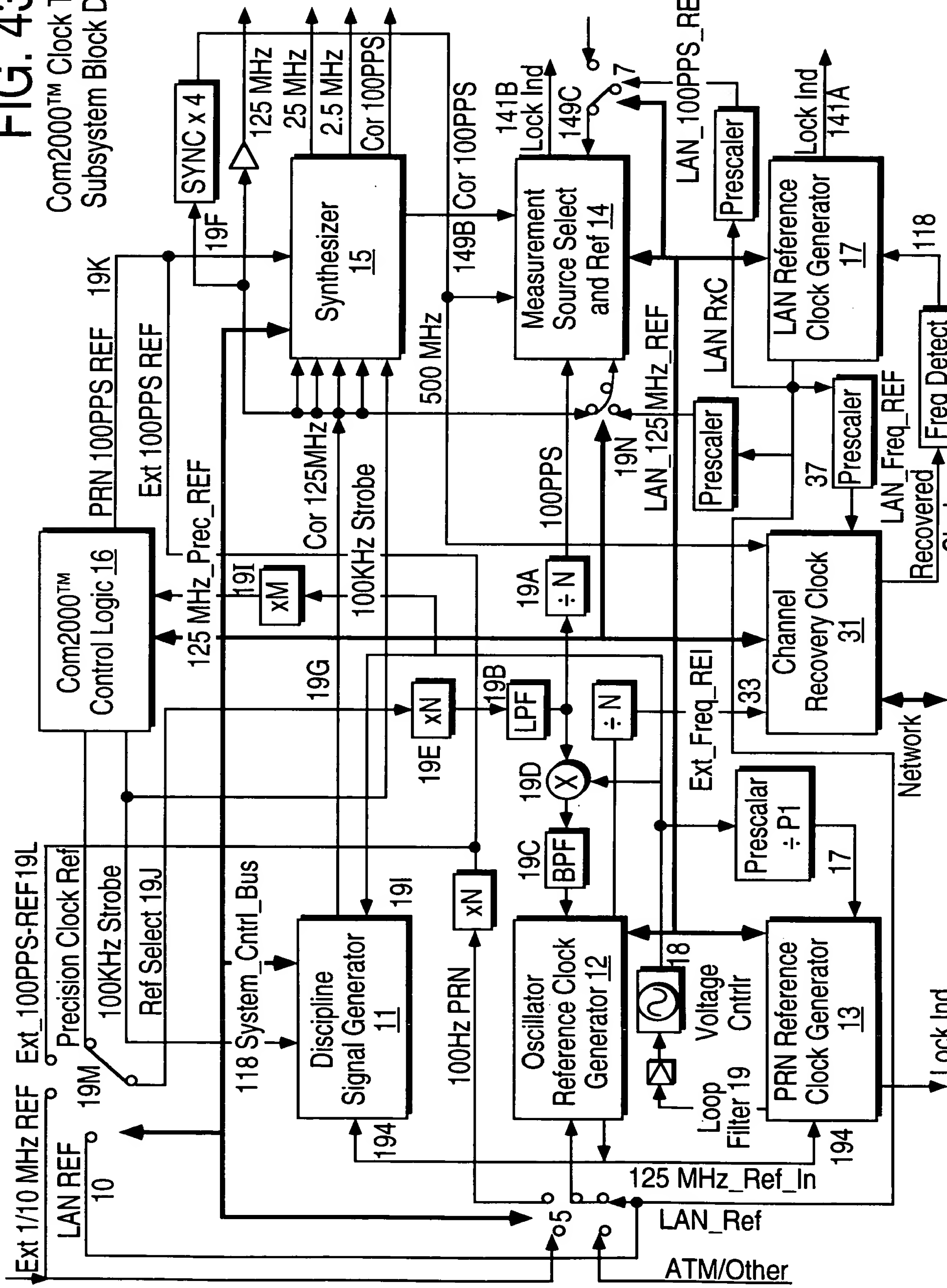
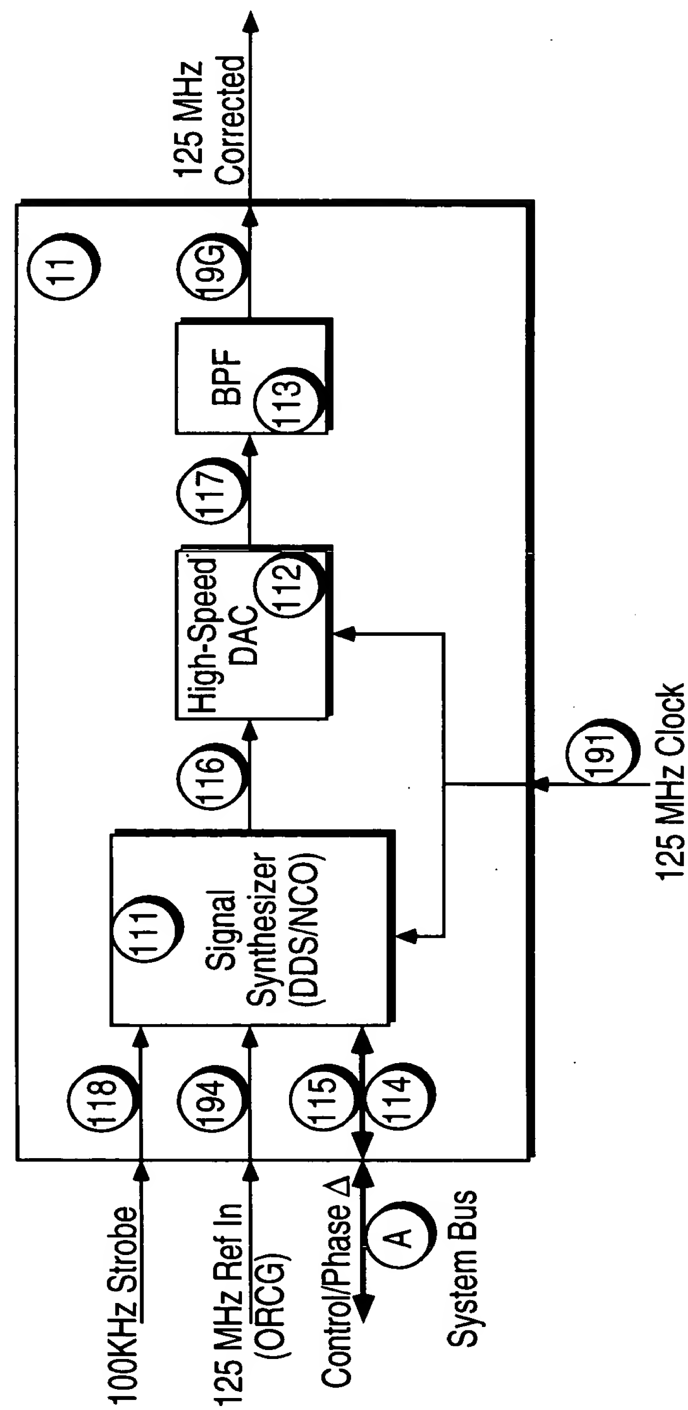


FIG. 43A
Discipline Signal Generator



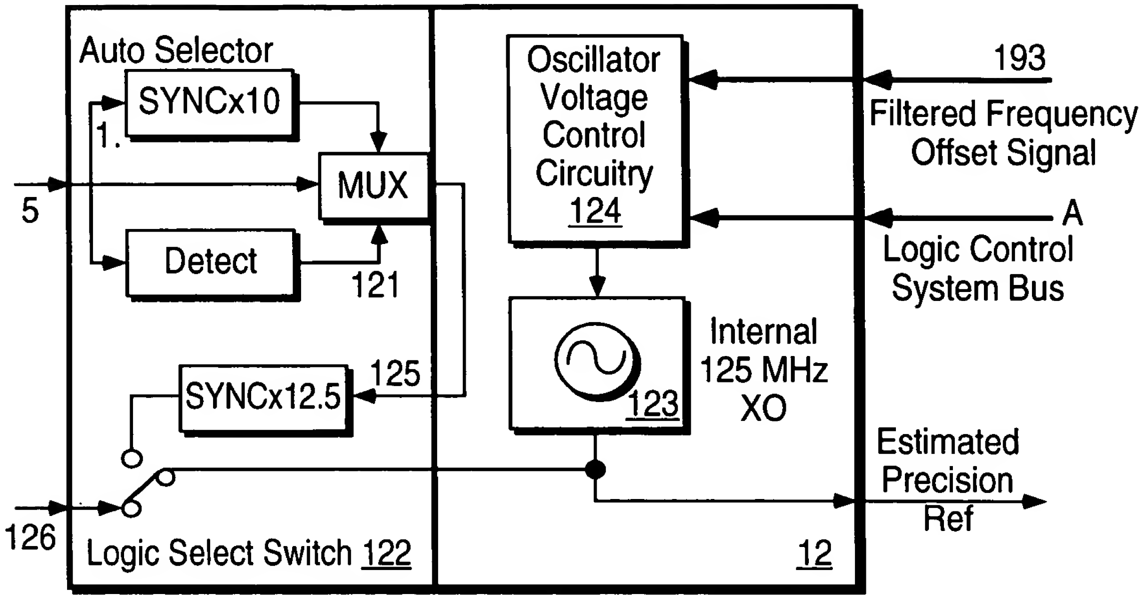


FIG. 43B
Oscillator Reference Clock Generator

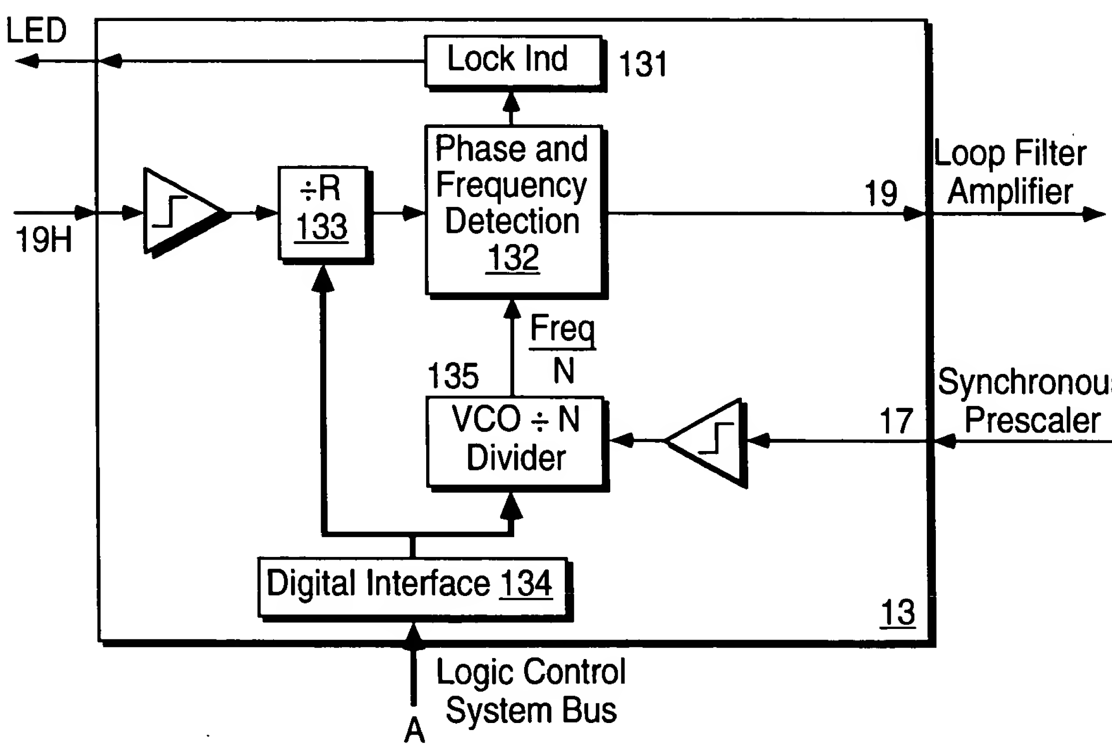


FIG. 43C
Precision Reference Clock Generator

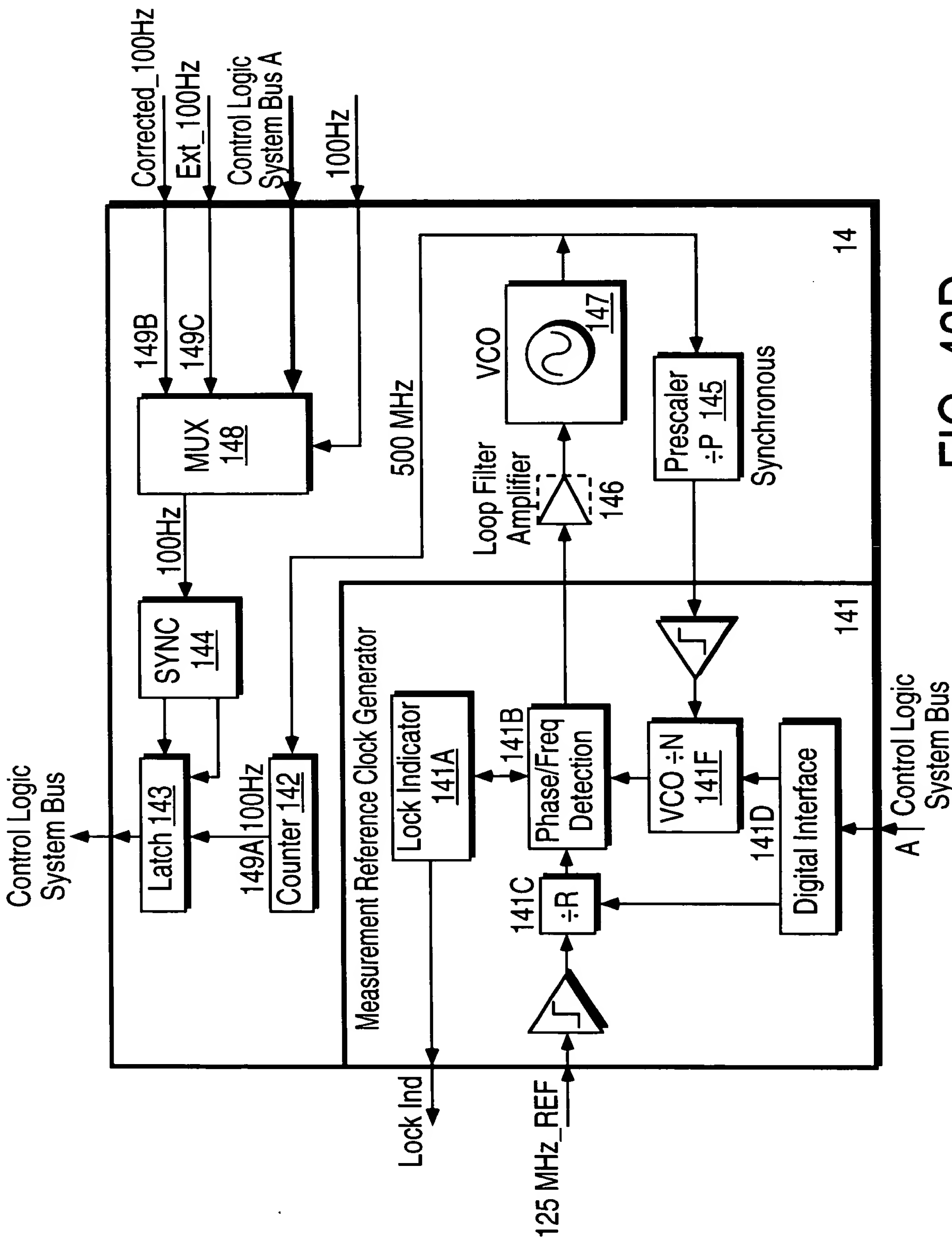


FIG. 43D
Measurement Source Selector

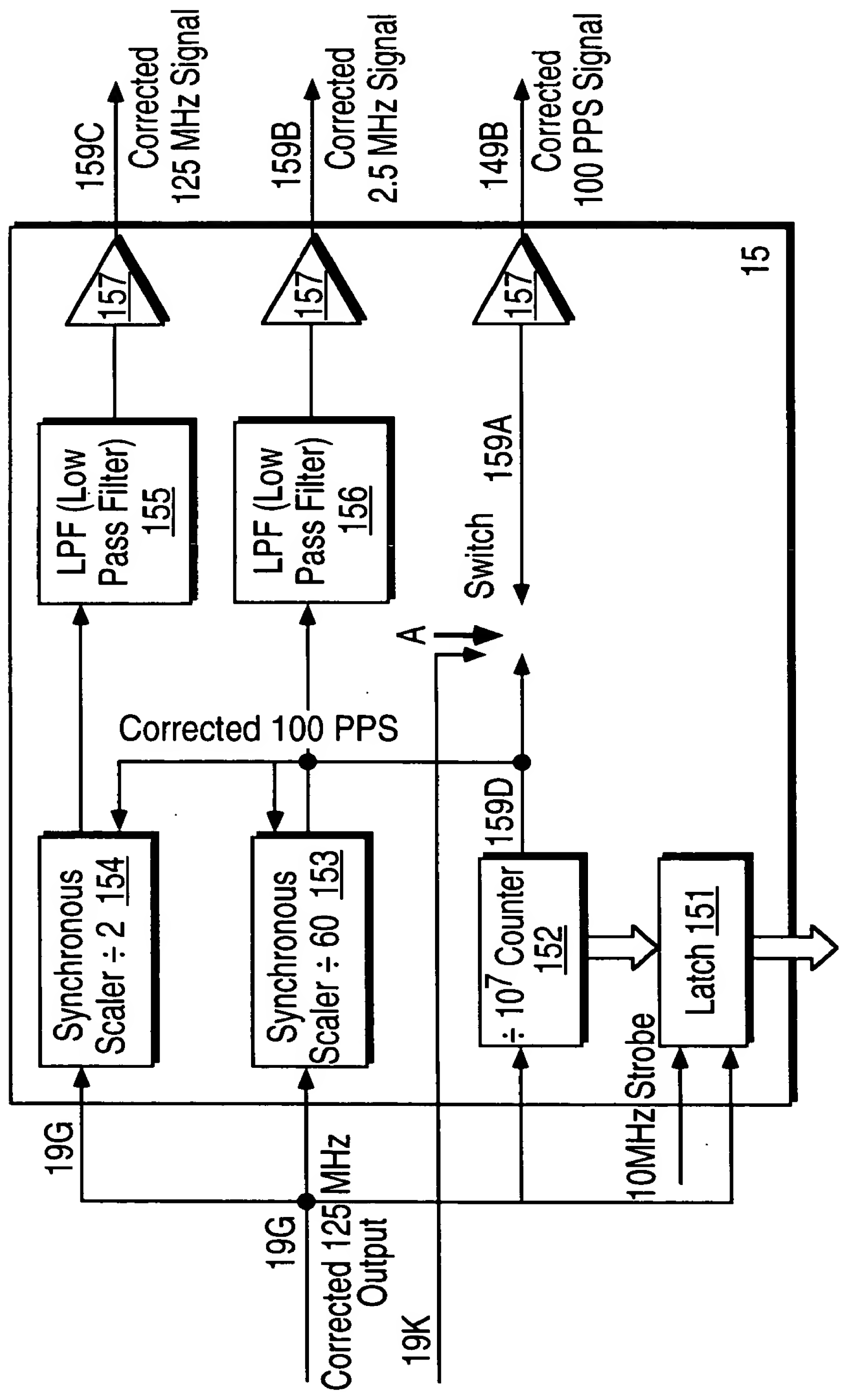


FIG. 43E
Corrected Output Generator

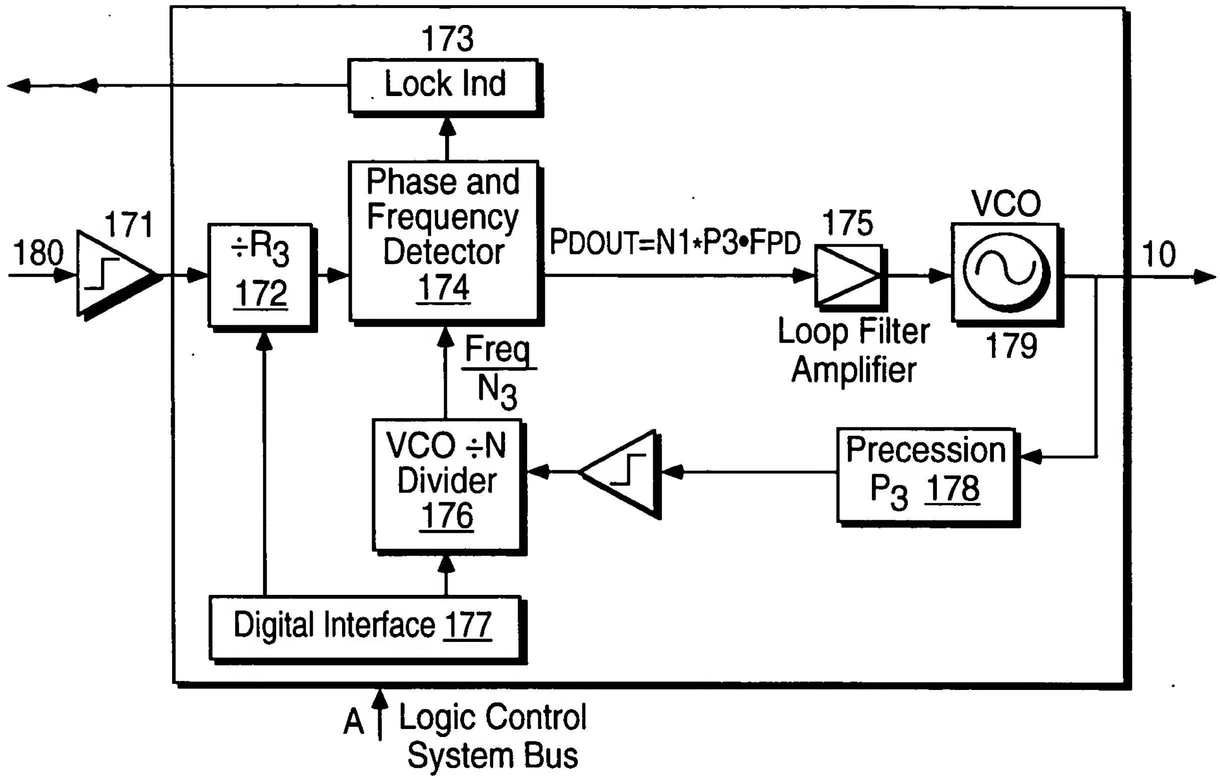


FIG. 43F
Com REF Clock Generator

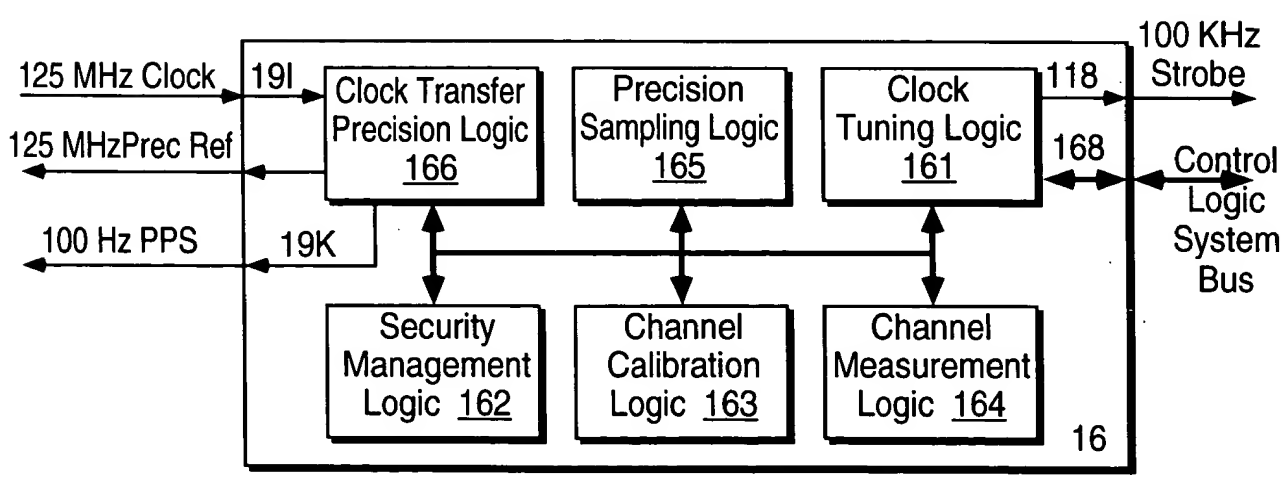


FIG. 44
Com 2000™ Clock Transfer Control Logic

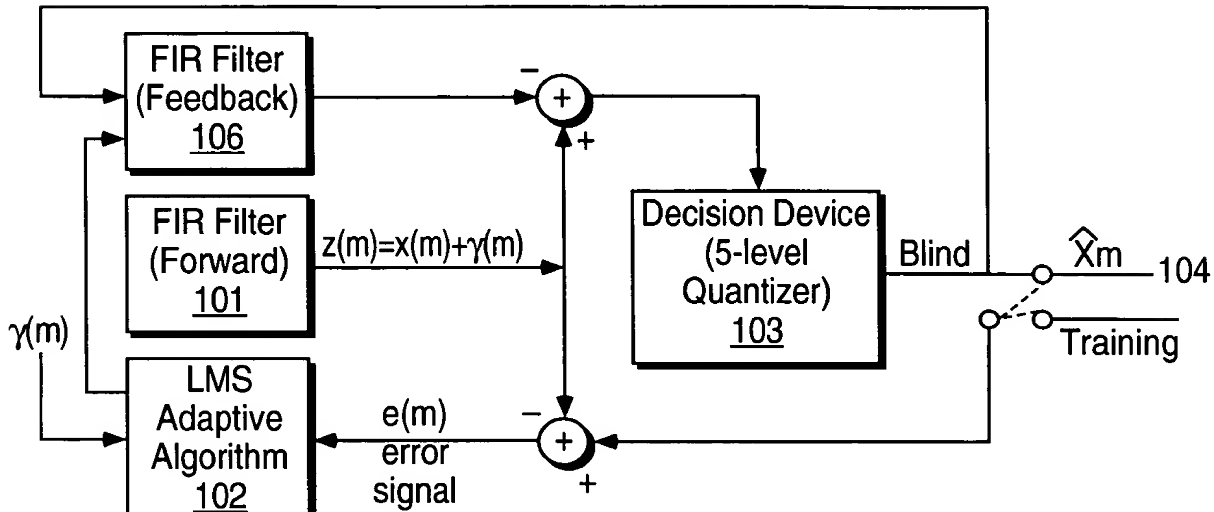


FIG. 45

Com2000™ LMS Adaptive Equalizer

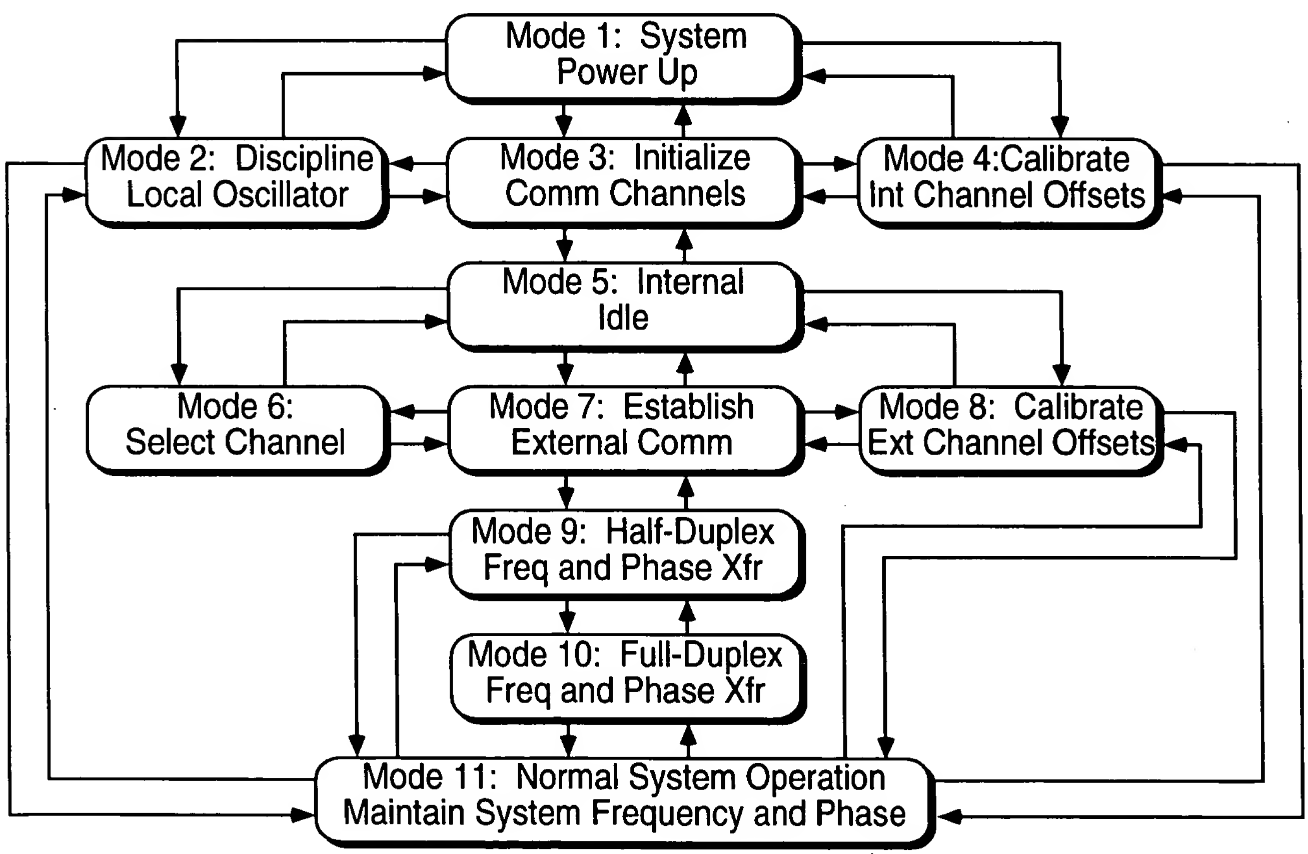


FIG. 46

Com 2000™ State Transition Diagram

FIG. 47A

High Level UnitNet System Block Diagram

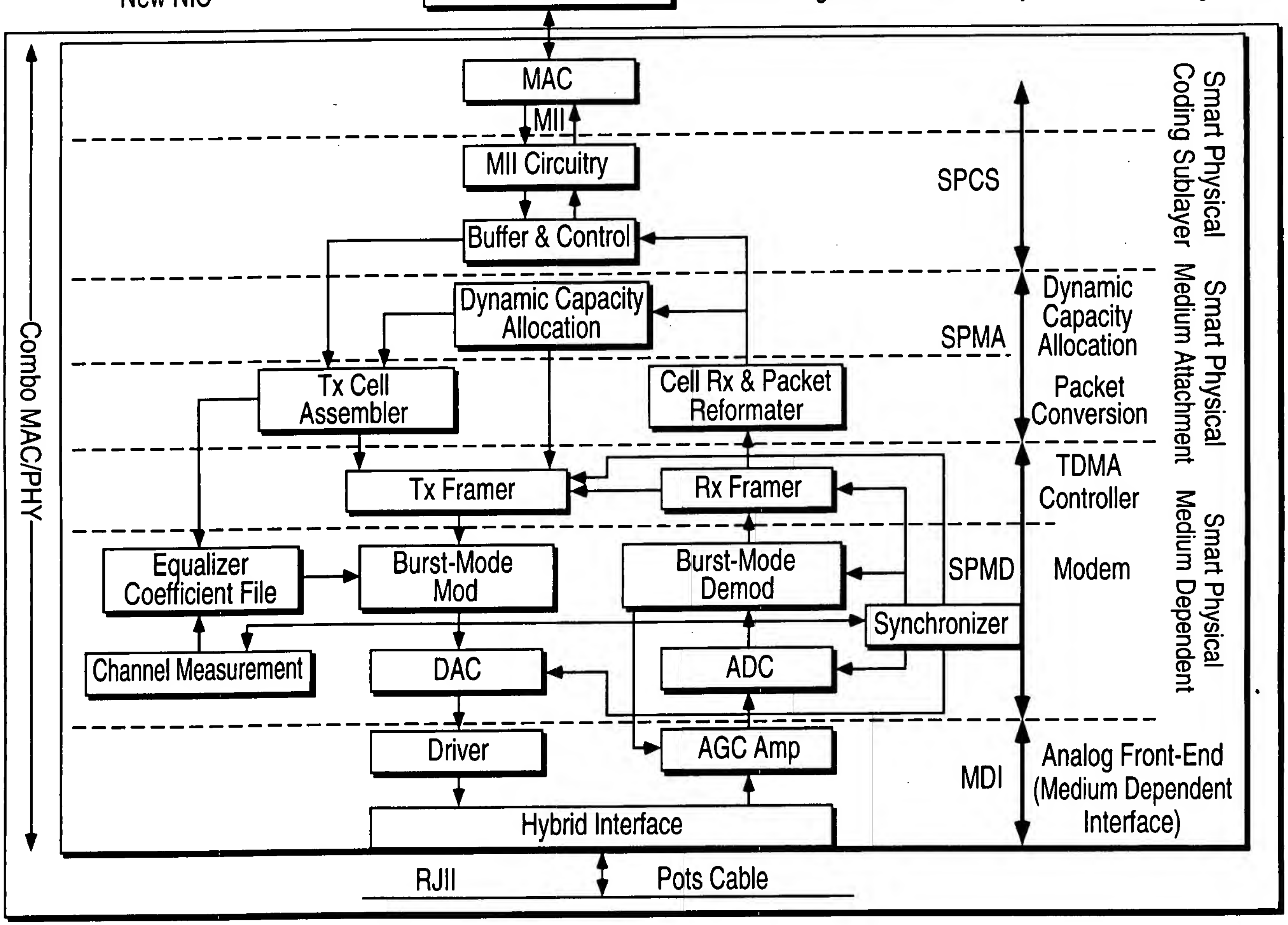
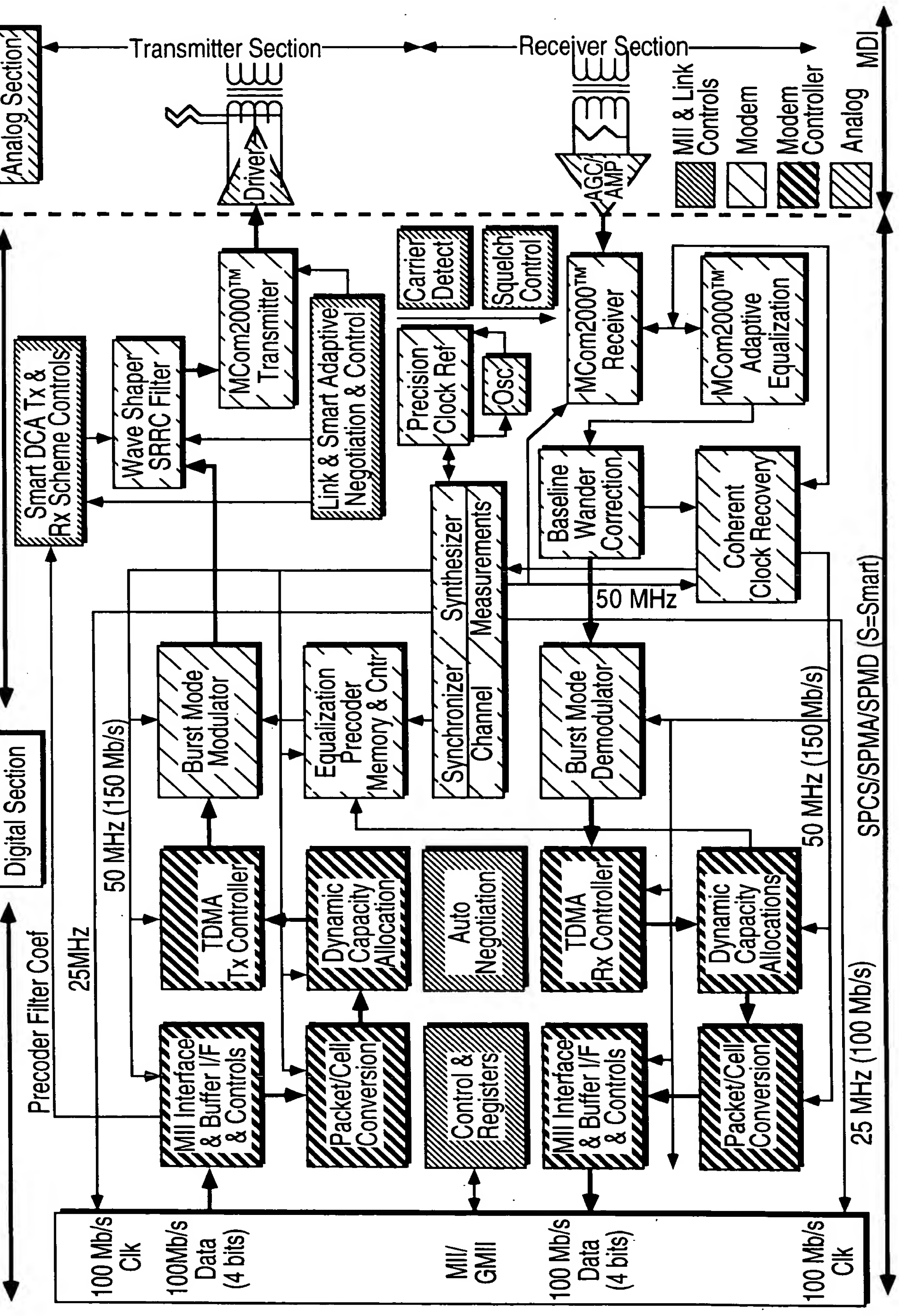


FIG. 47B UnitNet System Architecture Diagram



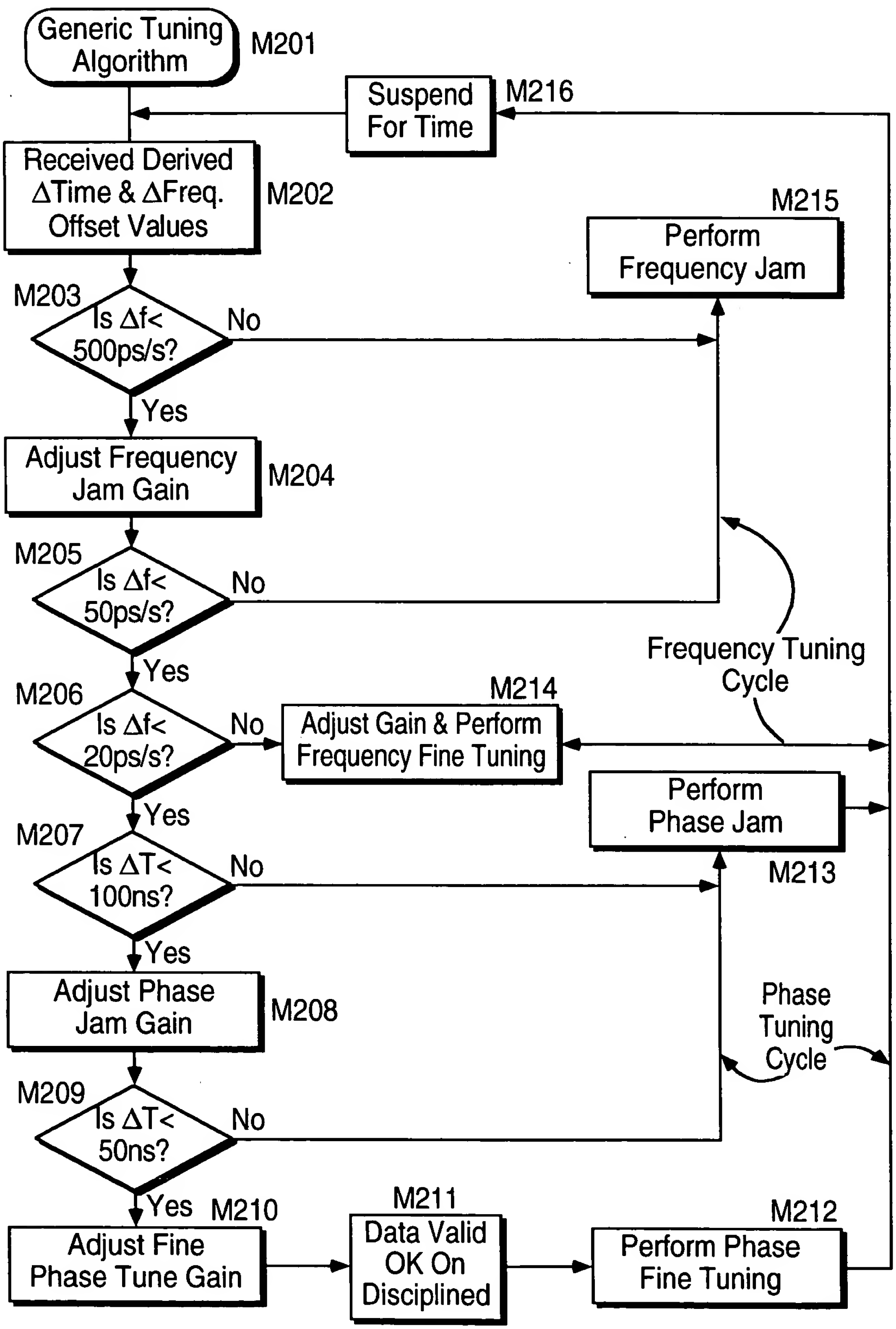
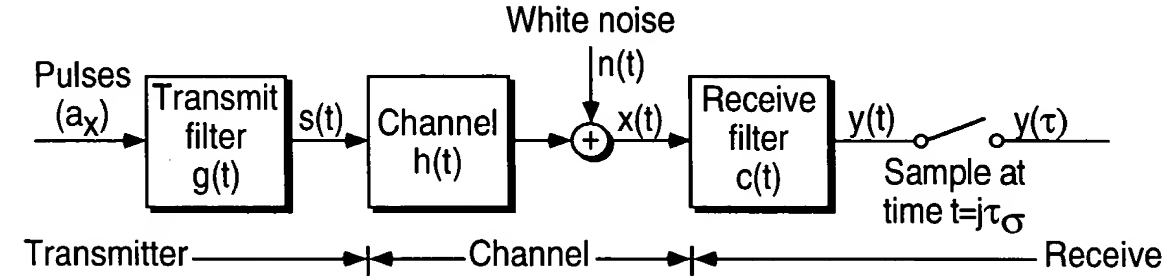


FIG. 48

Generic Tuning Algorithm

Intersymbol Interference



$s(t) - \sum_k a_k \sigma(t - K\tau_\sigma)$ $\mu\tau(t)\text{-}g(t)\text{-}h(t)\text{-}c(t)$ $y(t) - \mu\sum_k a_k \sigma(t - K\tau_\sigma) + n(t)$

The receiver filter output is sampled at time intervals $t_a = t\tau b$ giving

$$y(t_1) - \sum_{k=0}^{\infty} a_k P((t - K)T_0) + n(t_1)$$

$$- \mu\alpha_t + \mu\sum_{k=0}^{a} a_k P((i - K)T_0) + n(t_1)$$

FIG. 49
The ISI Definitions

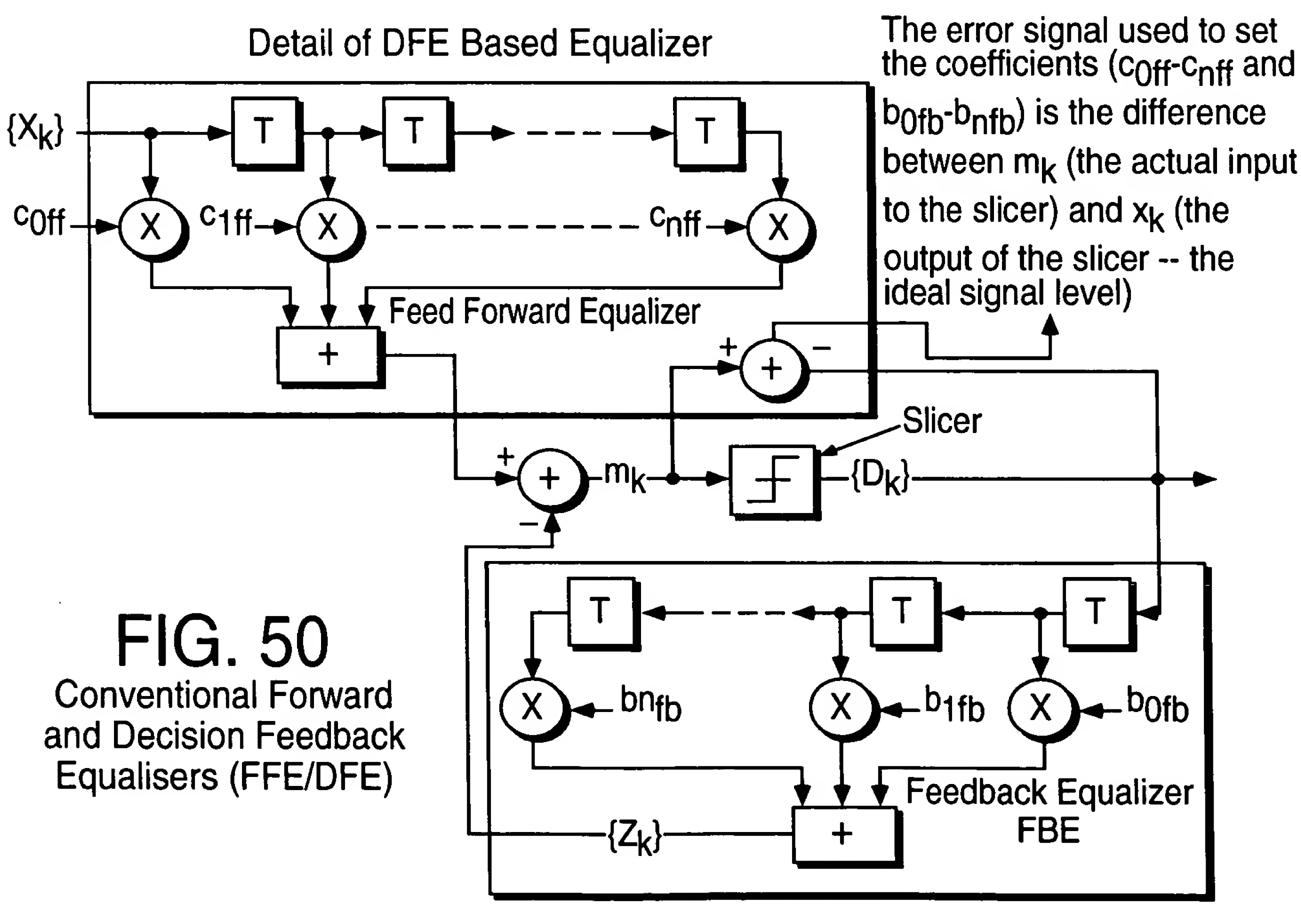


FIG. 50
Conventional Forward and Decision Feedback Equalisers (FFE/DFE)

(20*6.25 us or 10 nodes in the UniNet network), as shown in figure 05

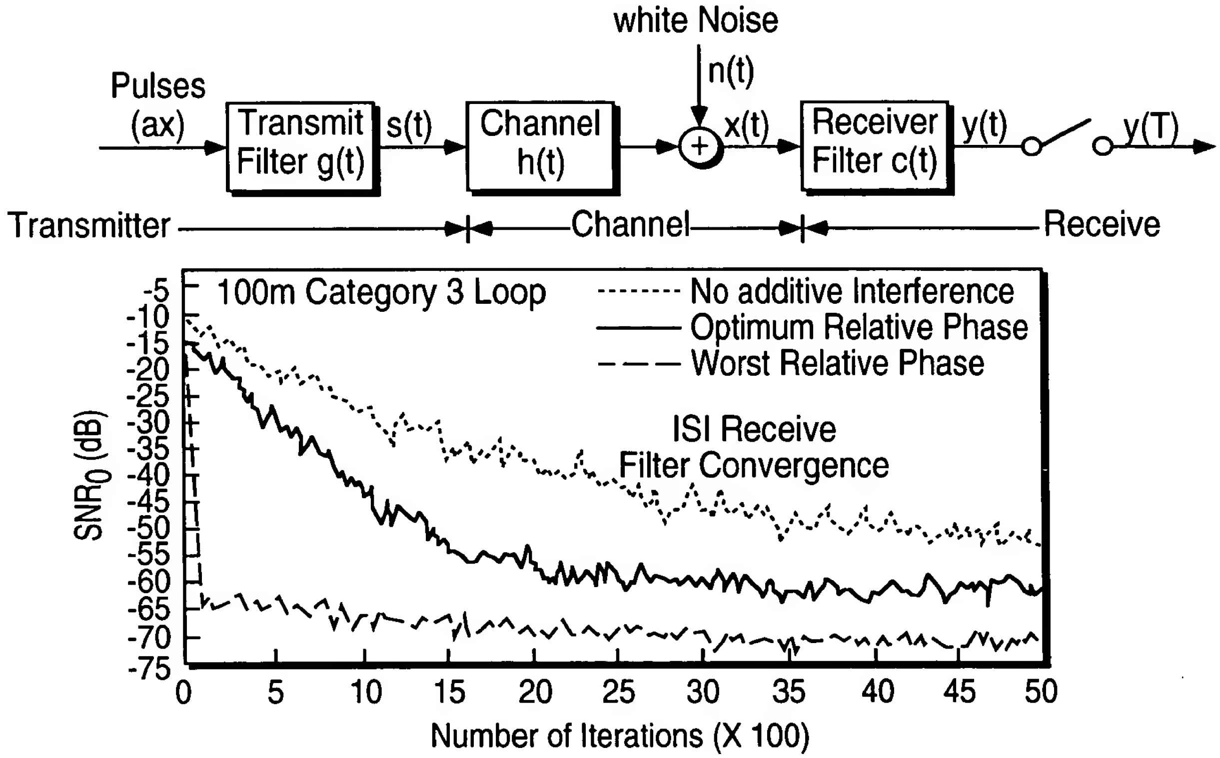


FIG. 51A

Phase Dependent Convergence of a FFE/DFE Filter

Performance of 51.84 Mb/s 16-CAP transceiver over 100 m category 3 cable with one cyclostationary NEXT interferes

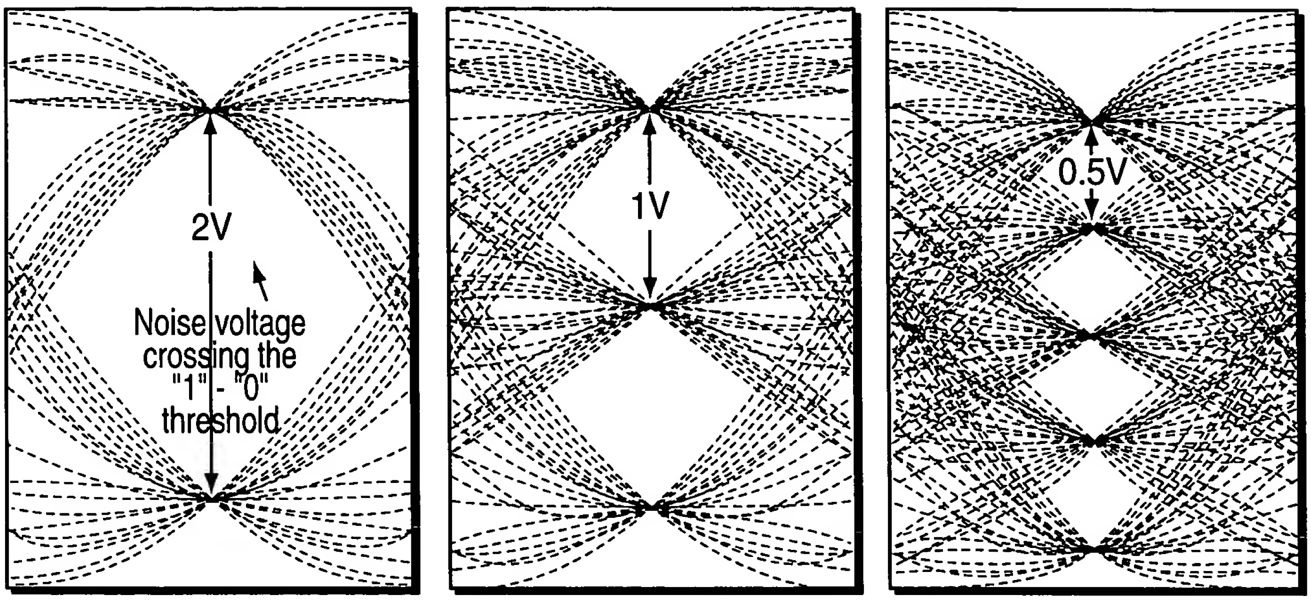
TIA/EIA NEXTR model a = 1.2 1/T = 12.96 Mbauch $P_2 = 10^{-10*}$

$\phi 1$ (i T/δ)	SNR_i (dB)	SNR_1 (dB)	SNR_n (dB)	Margin (dB)
ϕ_0	12.5	13.0	54.9	31.65
ϕ_1	12.5	14.8	58.1	43.85
ϕ_2	12.5	18.3	61.3	38.05
ϕ_3	12.5	18.4	61.9	38.65
ϕ_4	12.5	14.8	60.5	37.35
ϕ_5	12.5	13.0	57.1	33.85

*Margins are with respect to $P_2 = 10^{-10}$ for which $SNR_{0,mf}$ = 23.23 dB

FIG. 51B

Phase Dependent Convergence of FFE/DFE Filter - SNR



20 Log (1V/2V) = 6 dB degradation

20 Log (0.5V/2V) = 12 dB degradation

FIG. 52A

The Eye Open Diagram of Biphase Manchester, MLT3 and PAM5

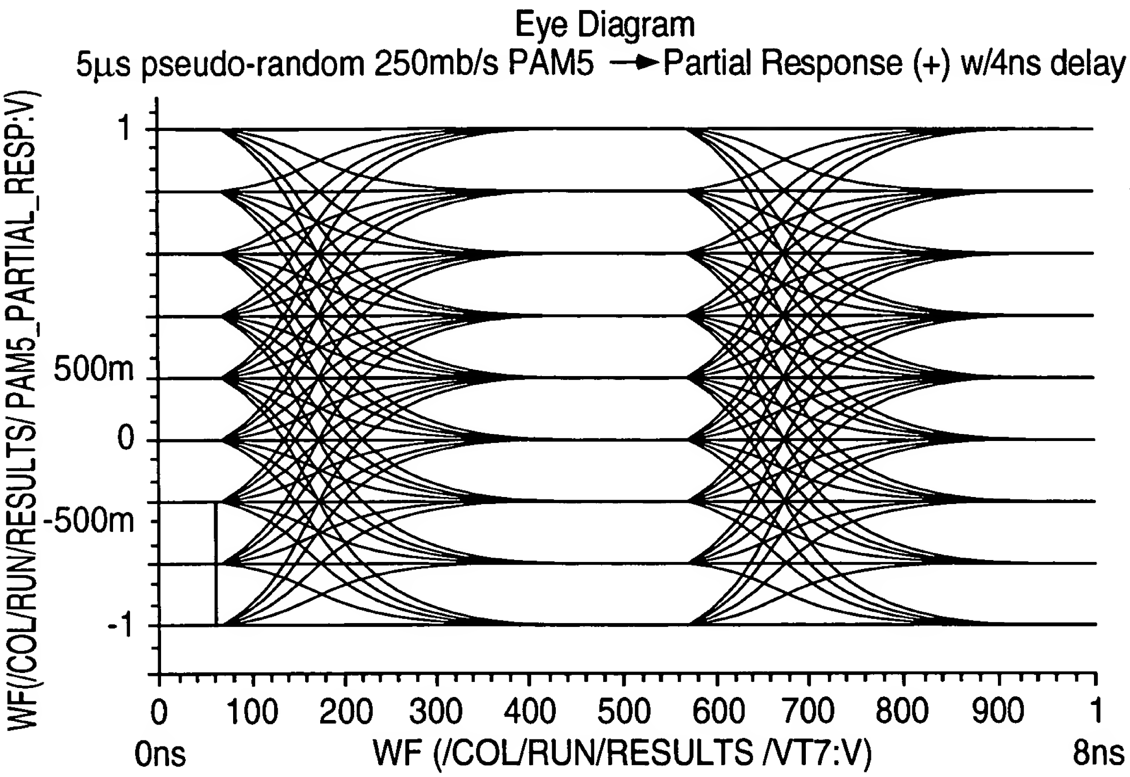


FIG. 52B

The Signal Spectrum and Eye Open Diagram of SPAM5

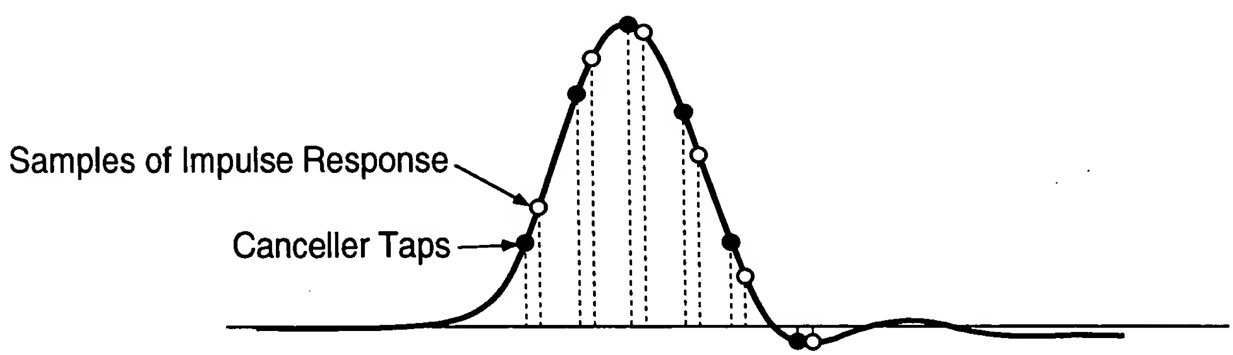


FIG. 53

The ECHO and NEXT Canceller Filter Performance

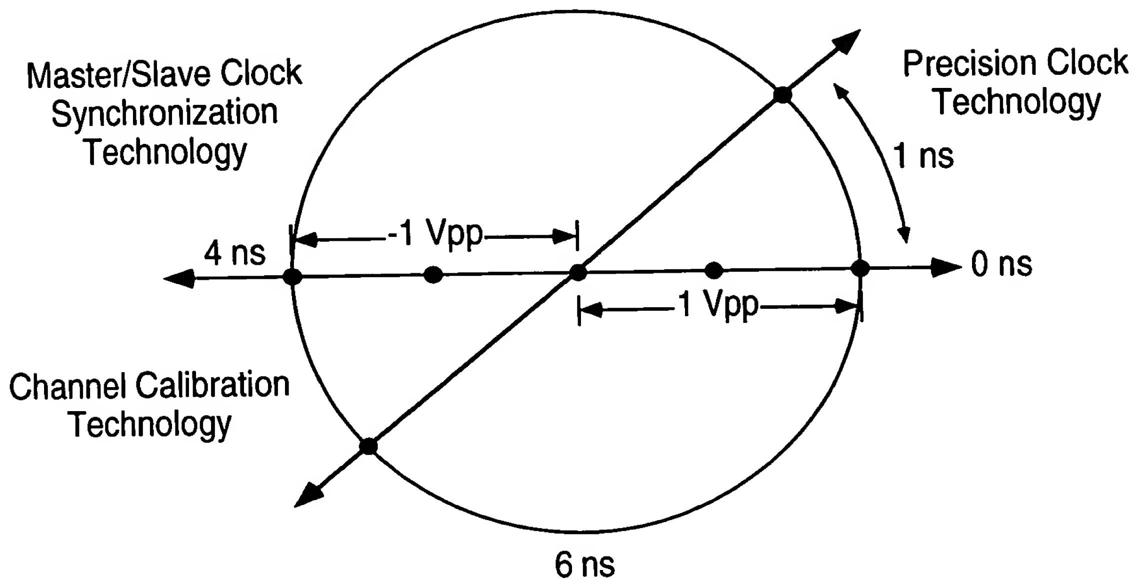


FIG. 54
Precision Phase Angle Controls

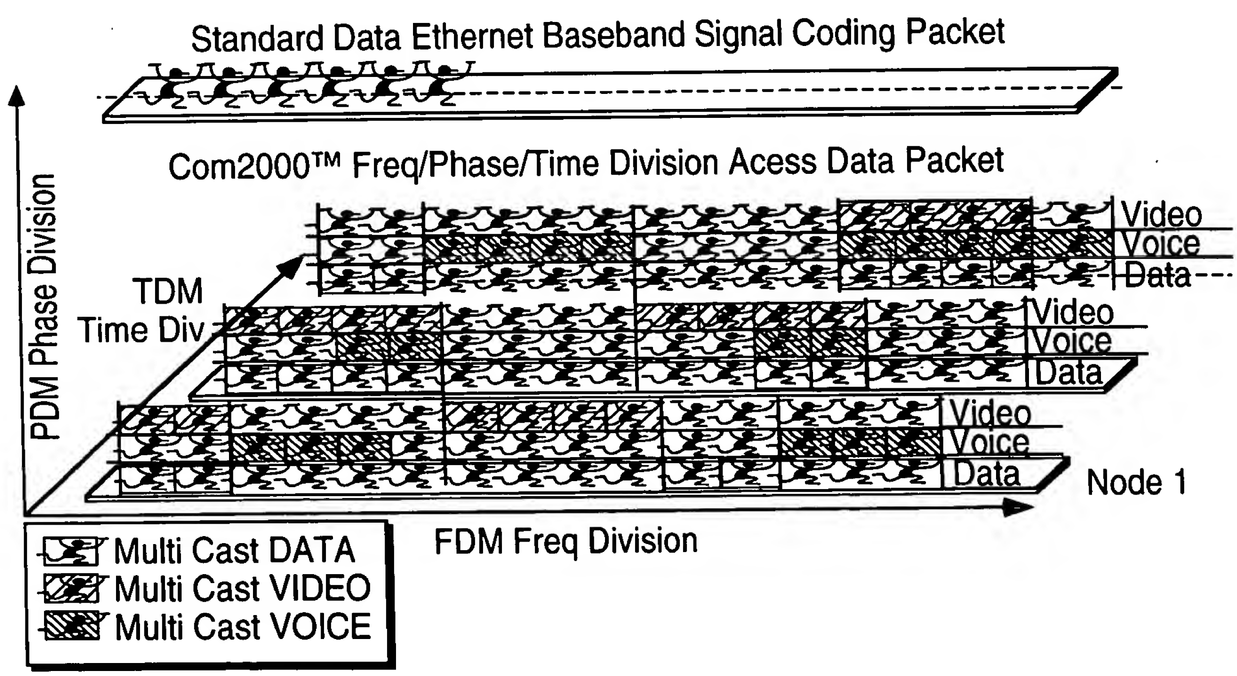
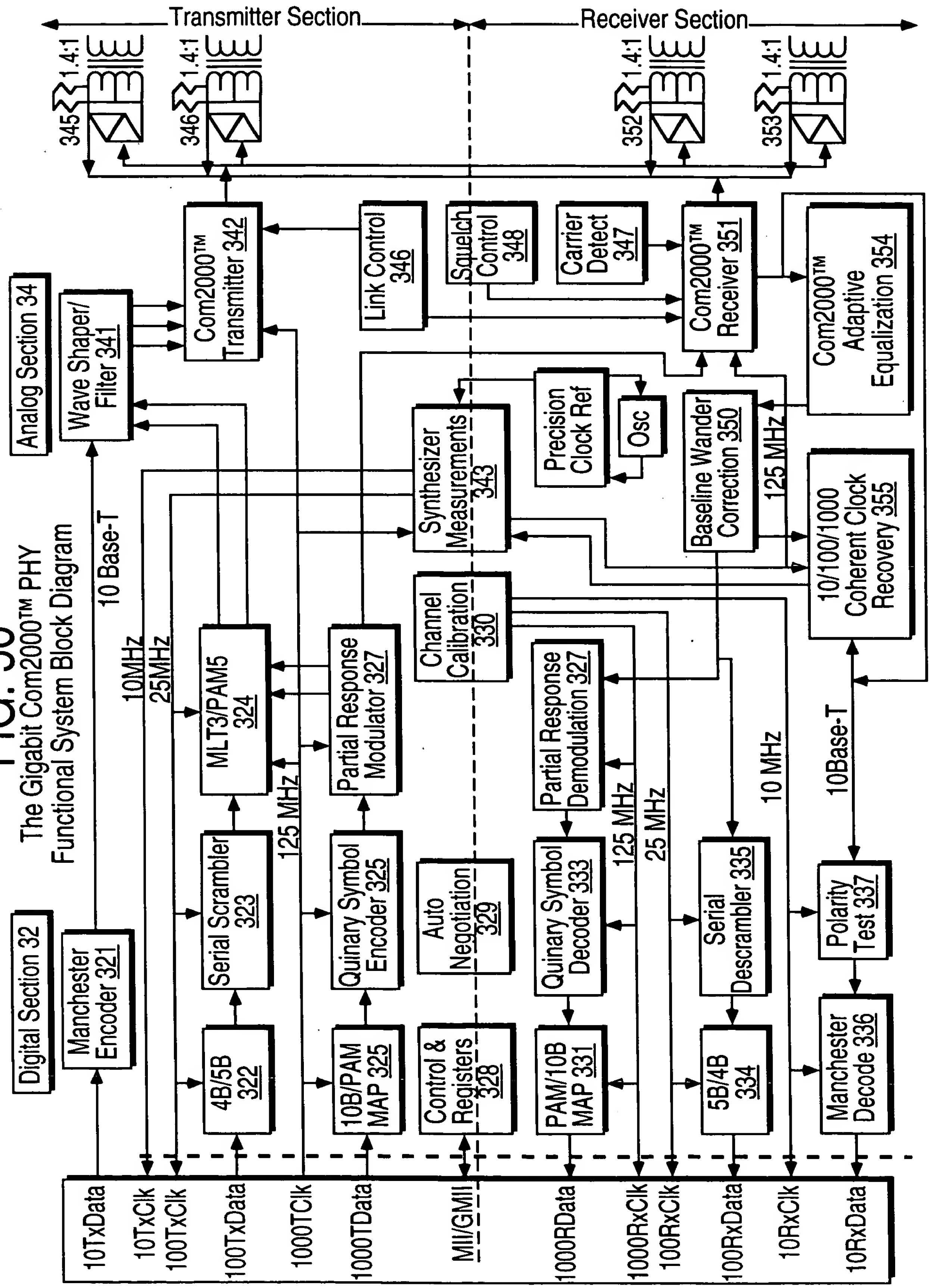


FIG. 55
Time, Phase, Frequency Division Multiple Access Signal Coding Scheme

Title: "Channel Equalization System And Method"
...ventors: Francois Trans & Tho Le-Ngoc
... Docket No.: 20870-06001; Case 6001 US
...ication No.: Not Yet Known
Sheet 61 of 97

FIG. 56
The Gigabit Com2000™ PHY
Functional System Block Diagram



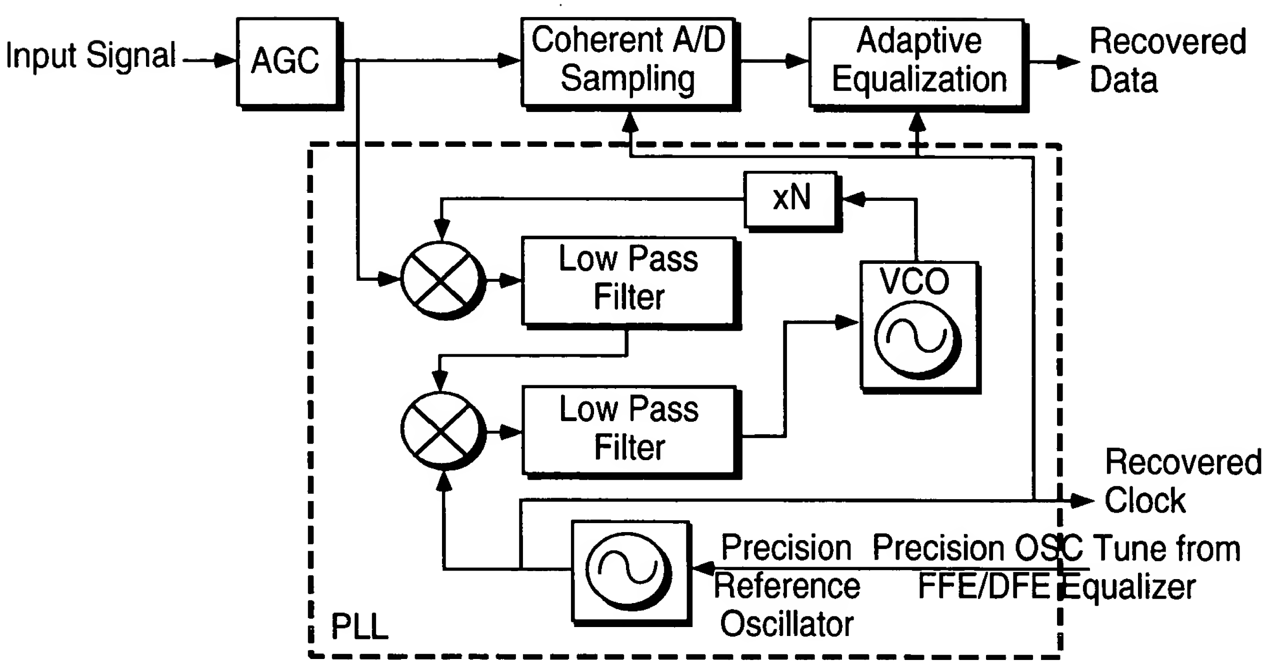


FIG. 57

Coherent Carrier Recover PLL Loop for UniNet Receiver

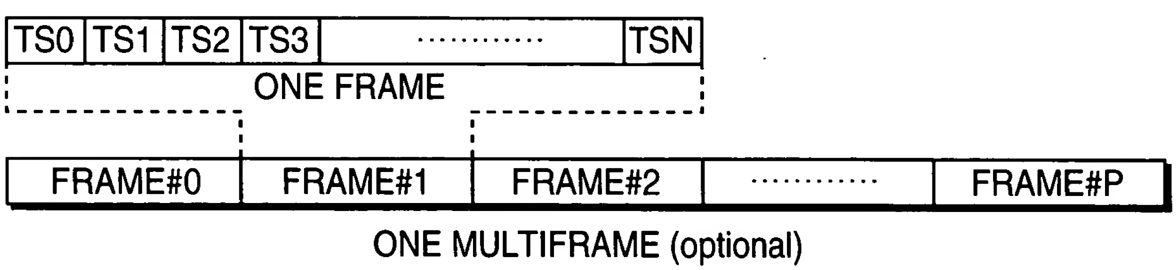


FIG. 58

General Frame Structures

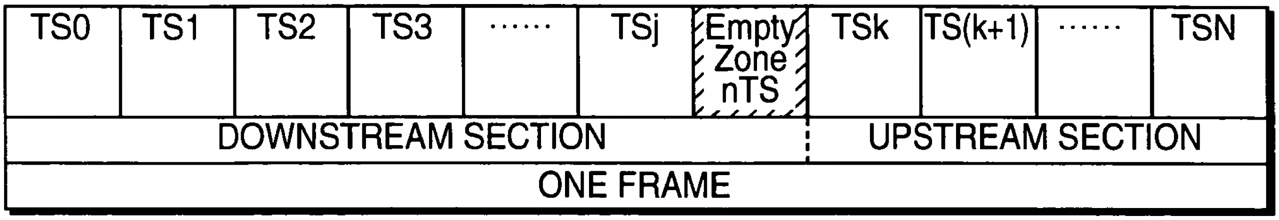


FIG. 59
Downstream and Upstream Sections

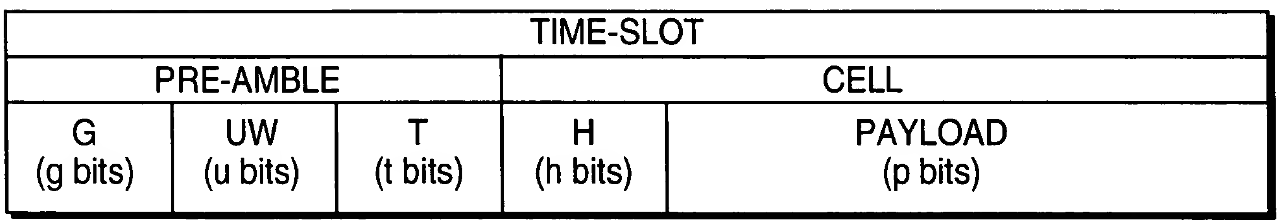


FIG. 60
Simplified Burst and Cell Structures

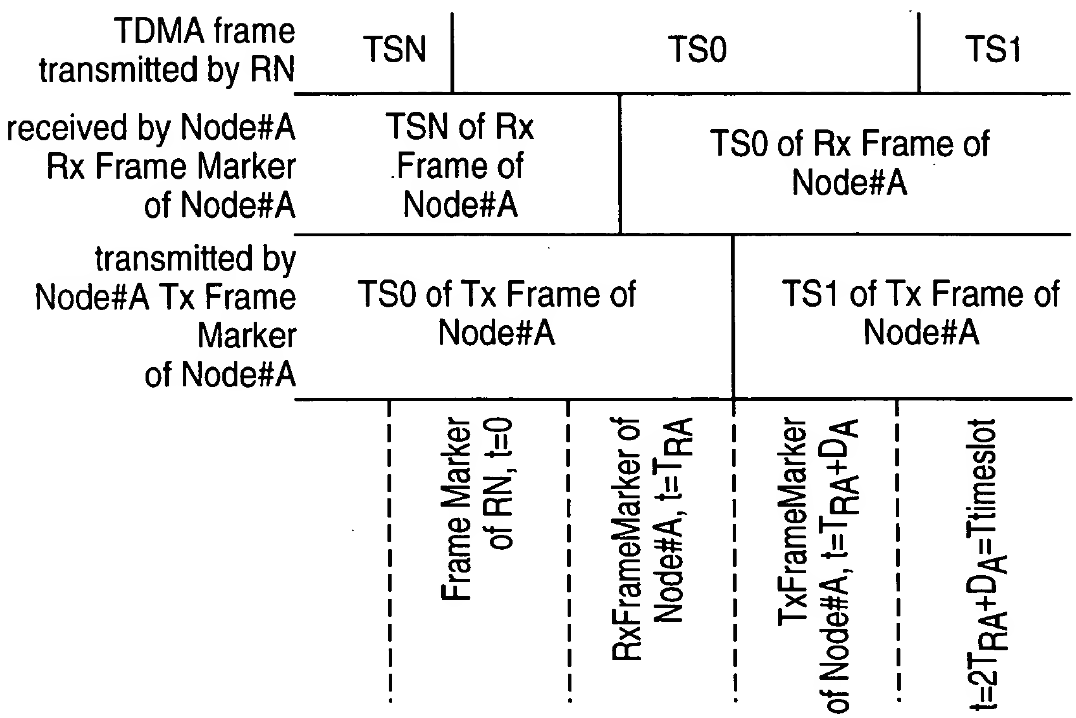


FIG. 61
Time Relationship between various Frame Markers

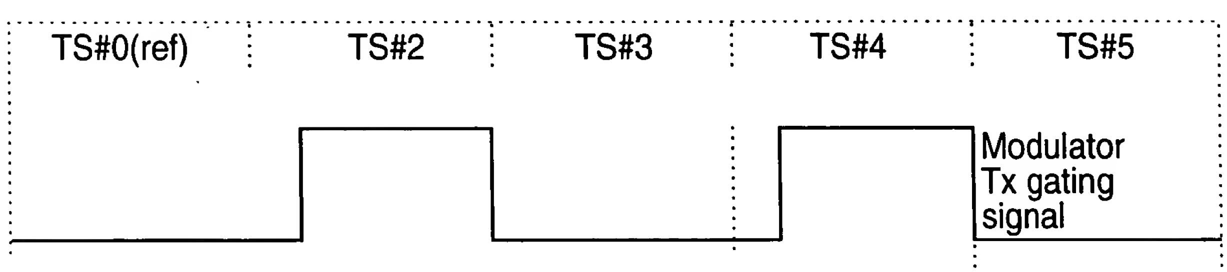


FIG. 62
Tx Frame Gating Signal

Sampling Phase or Error Vector Measurement (EVM)

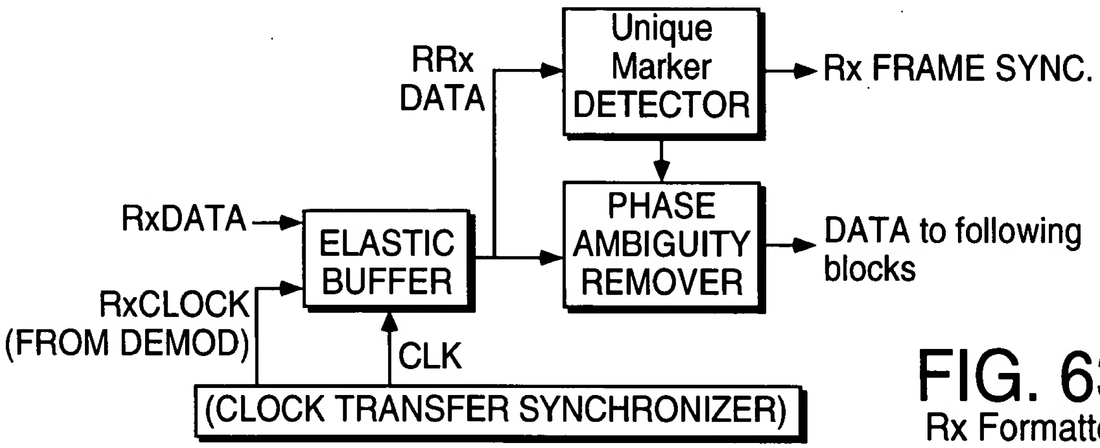


FIG. 63
Rx Formatter

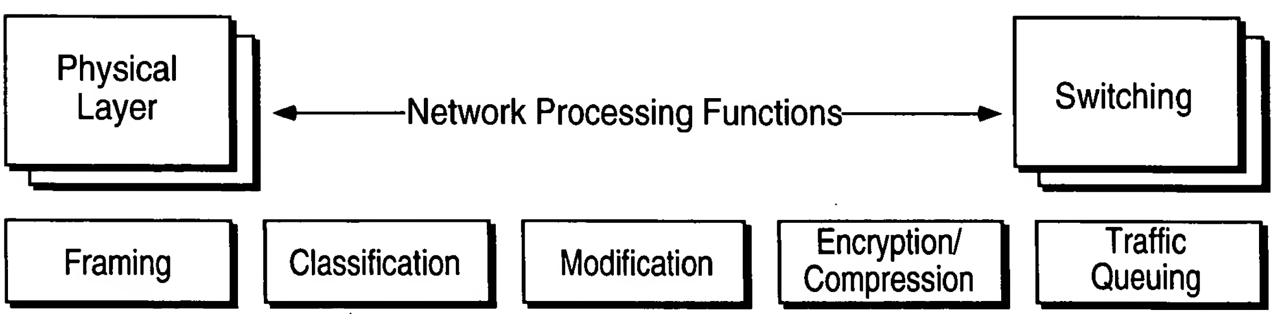


FIG. 64
IP Packet Network Processing Functions

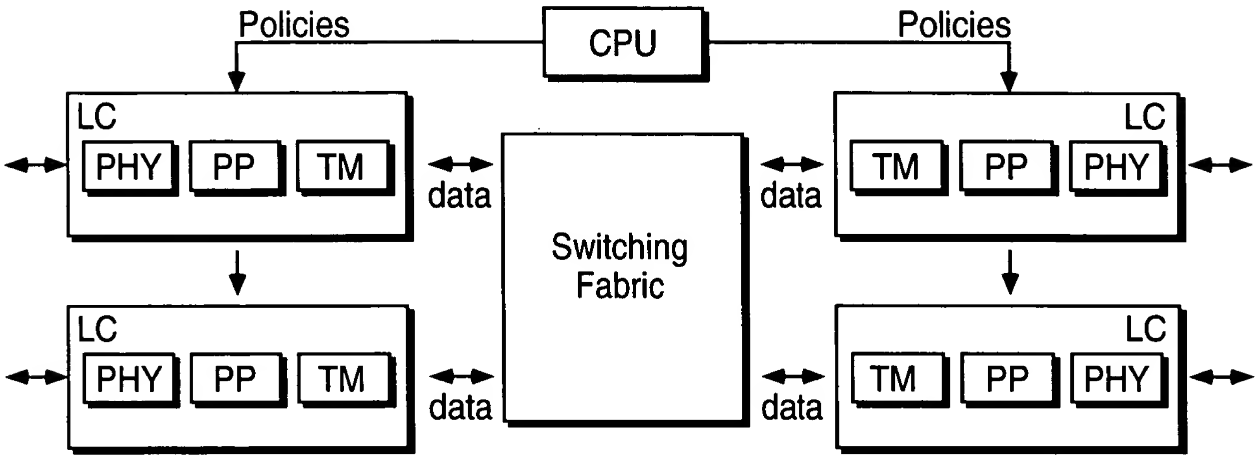


FIG. 65
Distributed Packet Switching Architecture

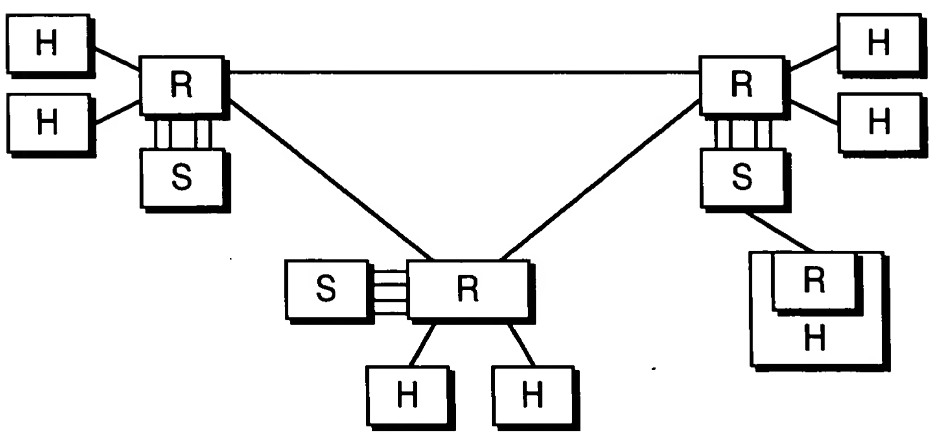


FIG. 66
UniNet Application over Existing Ethernet IP Networks

FIG. 67A/B

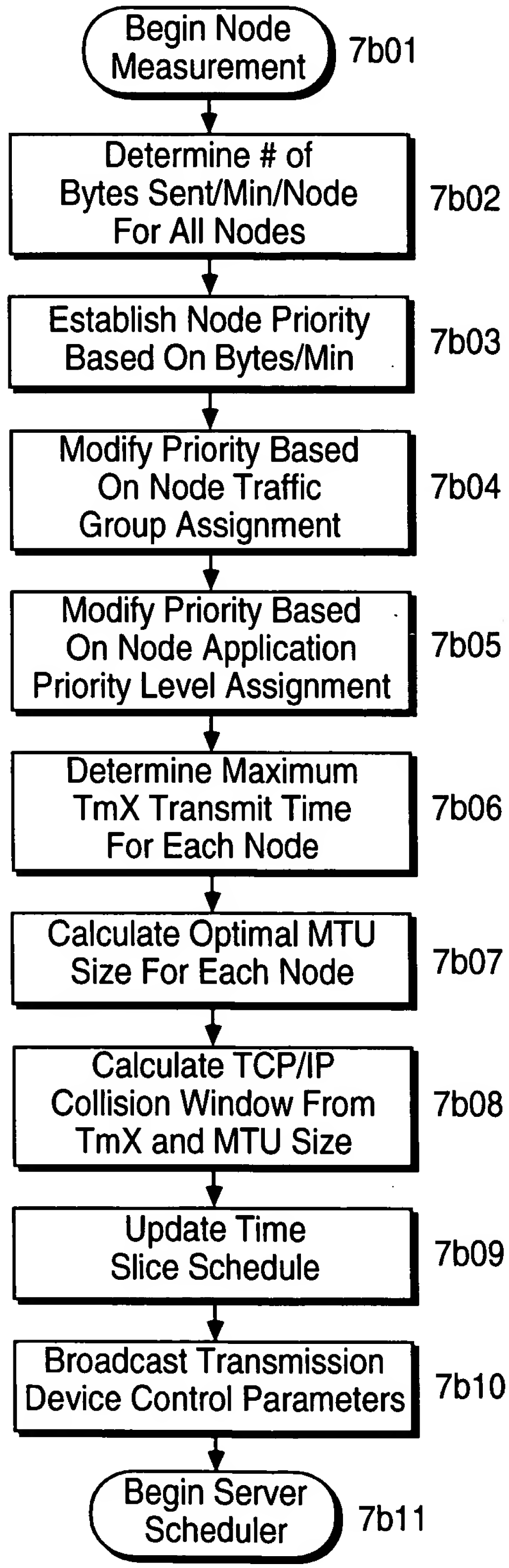

Begin Node Measurement
7b01
Determine # of Bytes Sent/Min/Node For All Nodes
7b02
Establish Node Priority Based On Bytes/Min
7b03
Modify Priority Based On Node Traffic Group Assignment
7b04
Modify Priority Based On Node Application Priority Level Assignment
7b05
Determine Maximum TmX Transmit Time For Each Node
7b06
Calculate Optimal MTU Size For Each Node
7b07
Calculate TCP/IP Collision Window From TmX and MTU Size
7b08
Update Time Slice Schedule
7b09
Broadcast Transmission Device Control Parameters
7b10
Begin Server Scheduler
7b11

FIG. 67C

DIPA/TDDA Algorithm

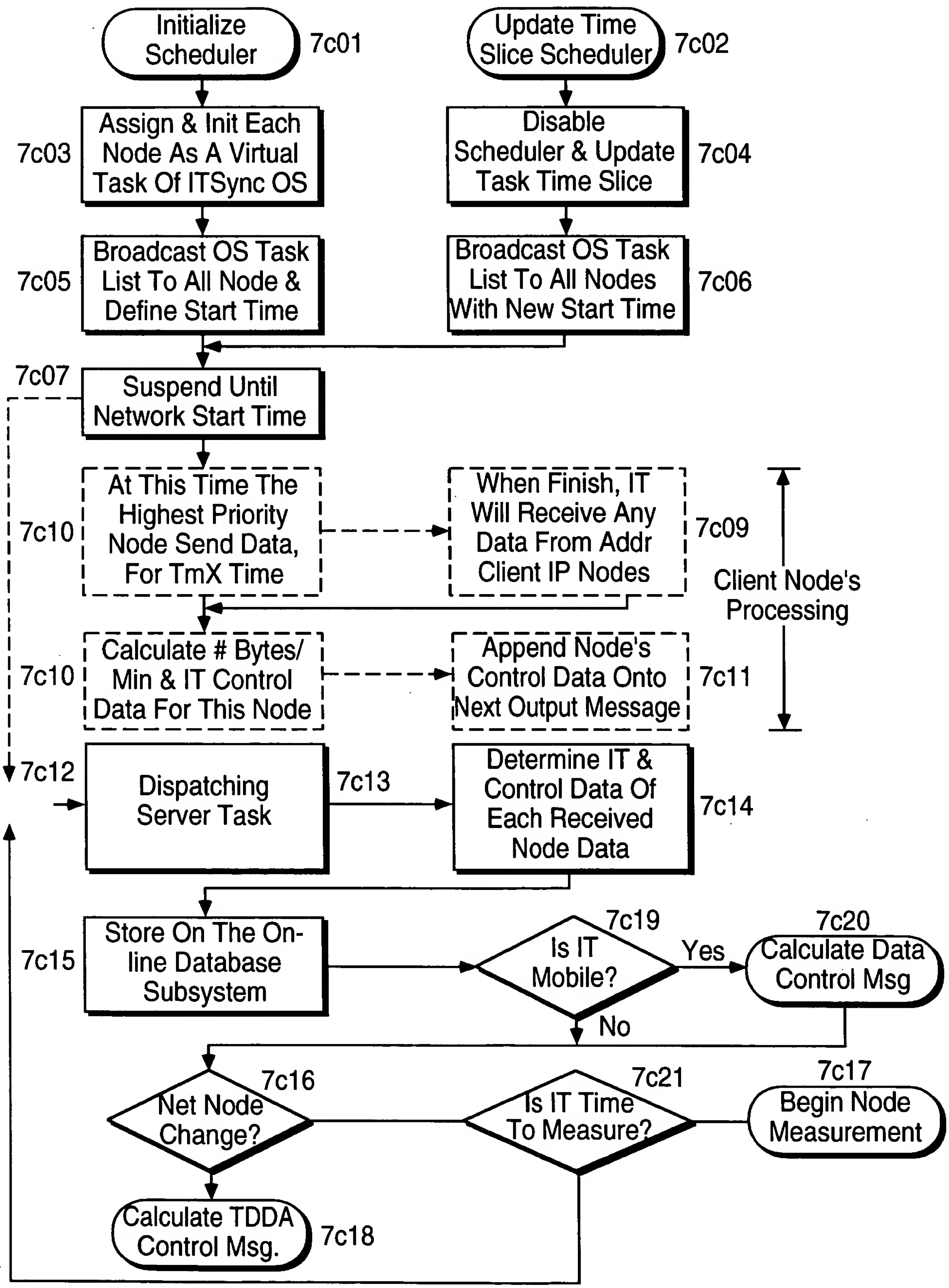


FIG. 67D
DIPA/TDDA Algorithm

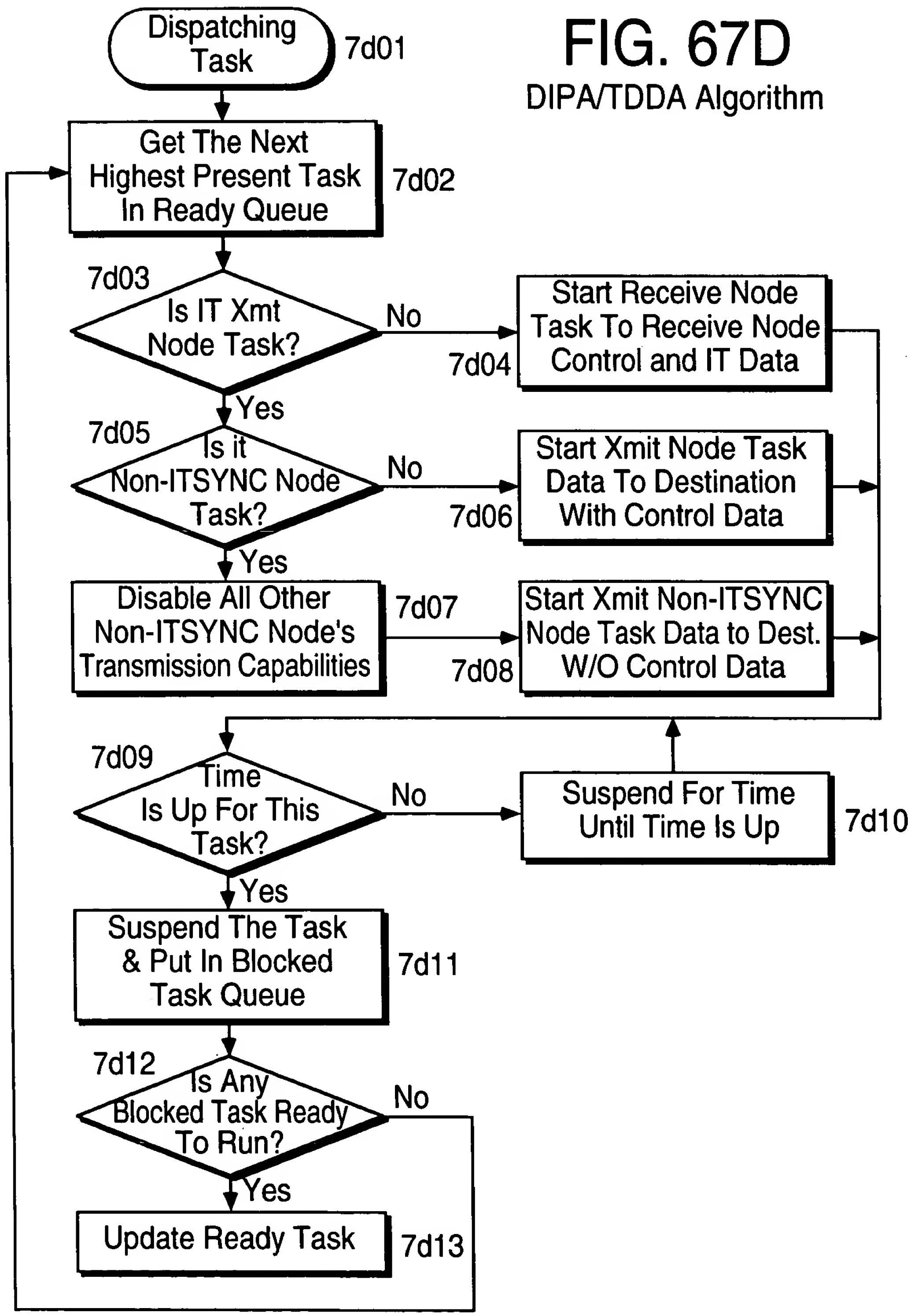


FIG. 67E

TDDA Algorithm

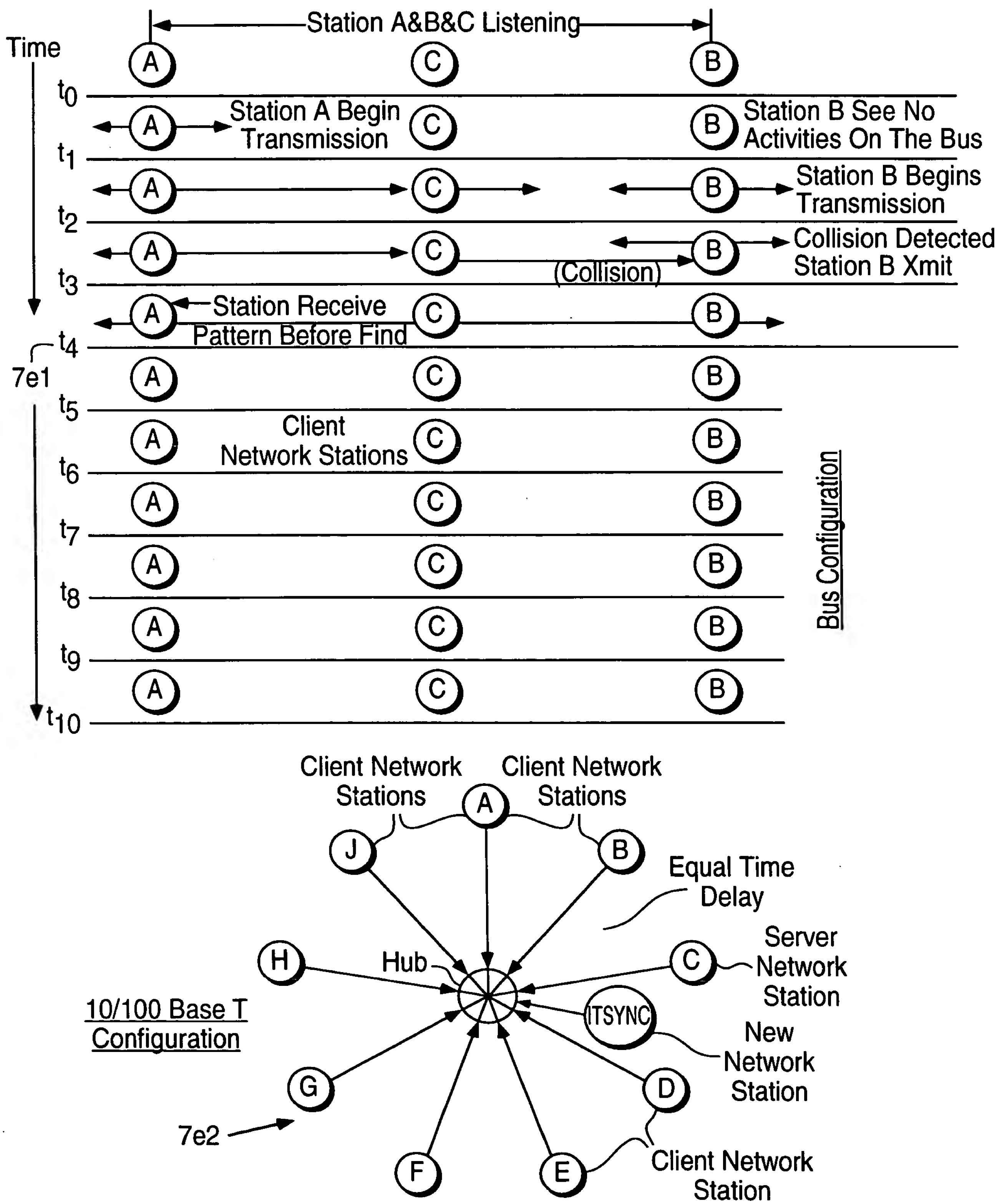
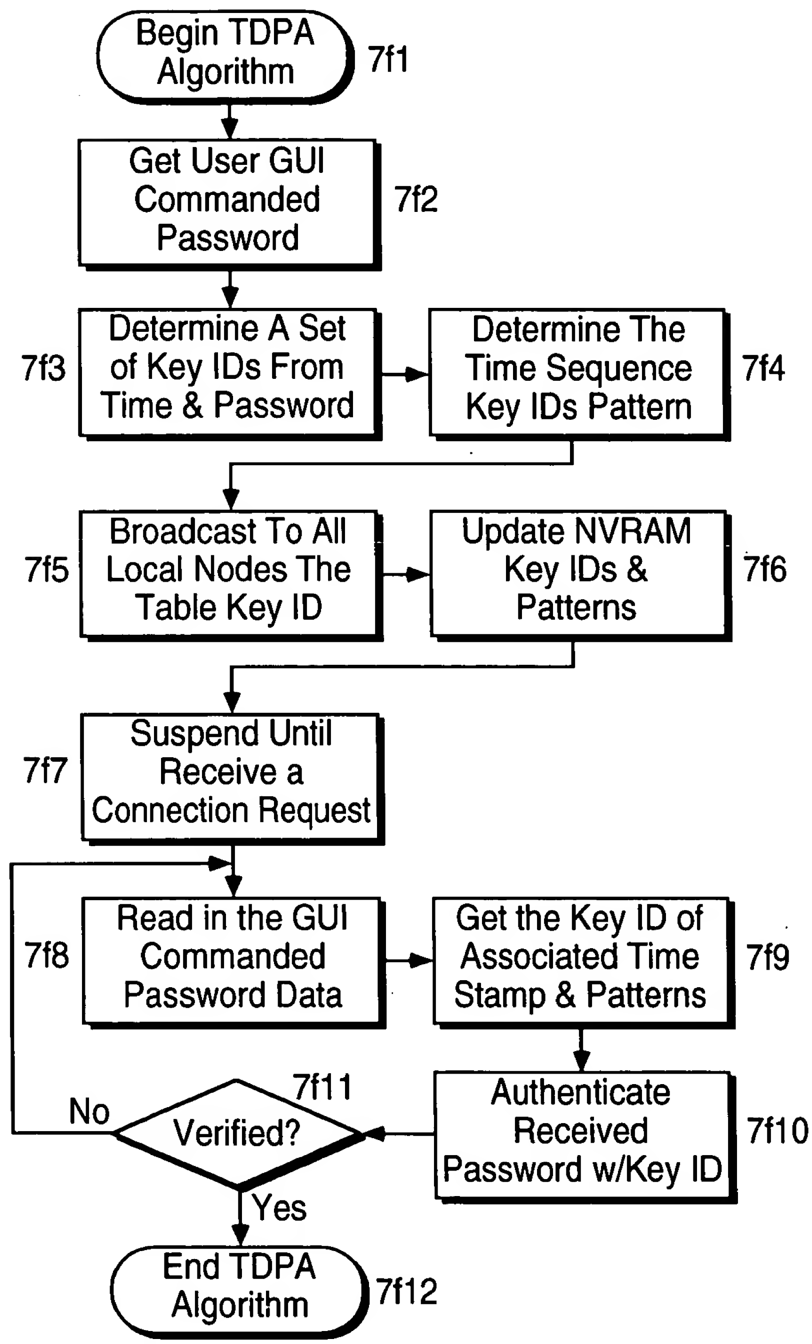


FIG. 67F

TDPA Algorithm



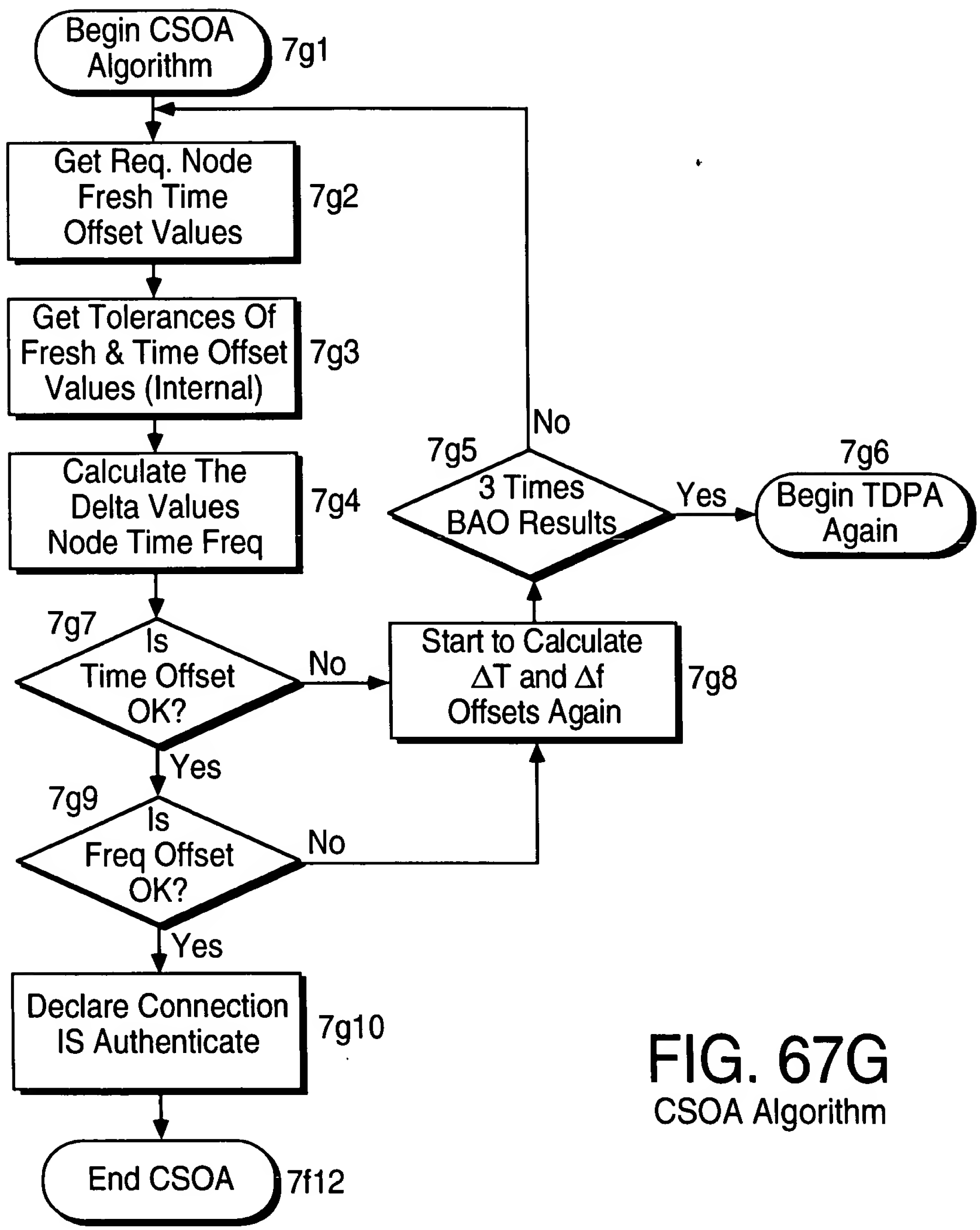


FIG. 67G
CSOA Algorithm

FIG. 67H/I

E-DNA Derived Key with 56 bits DES and Scrambled 64 Data bits

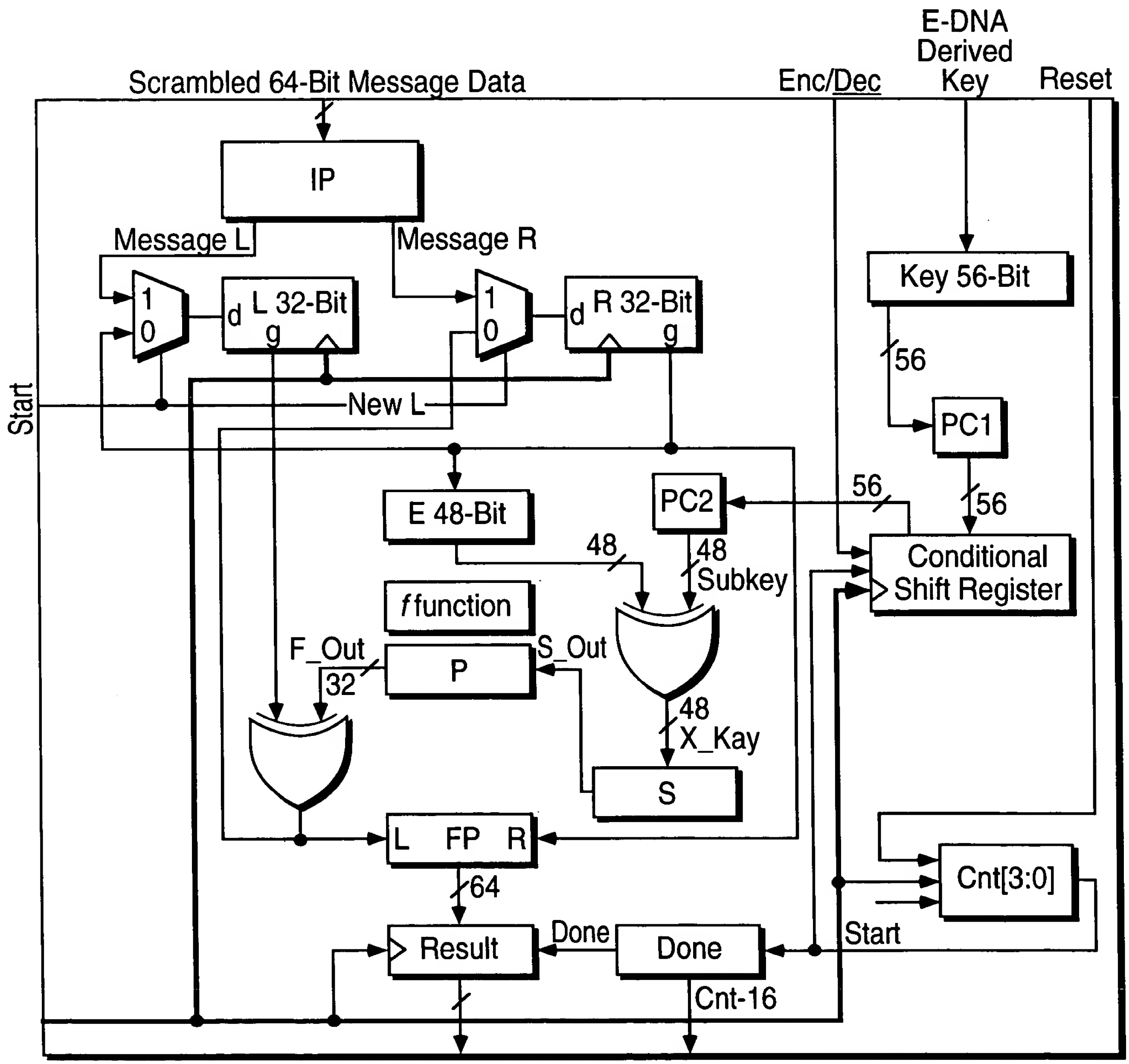


FIG. 67J/K

Expected Receiving Parameters Dependent DES Key Generation

E-DNA Key Encryption

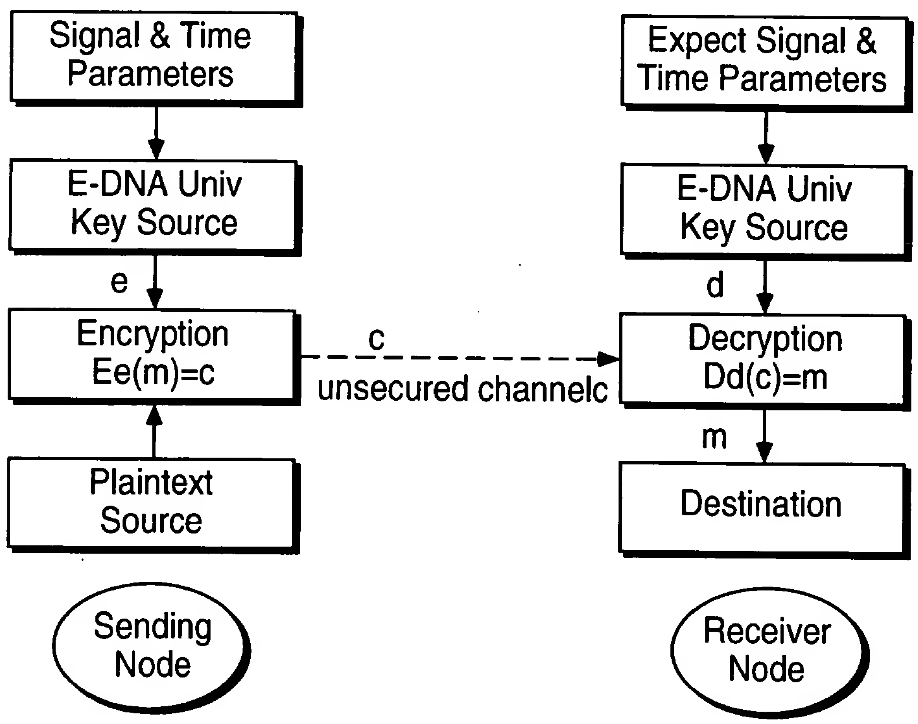
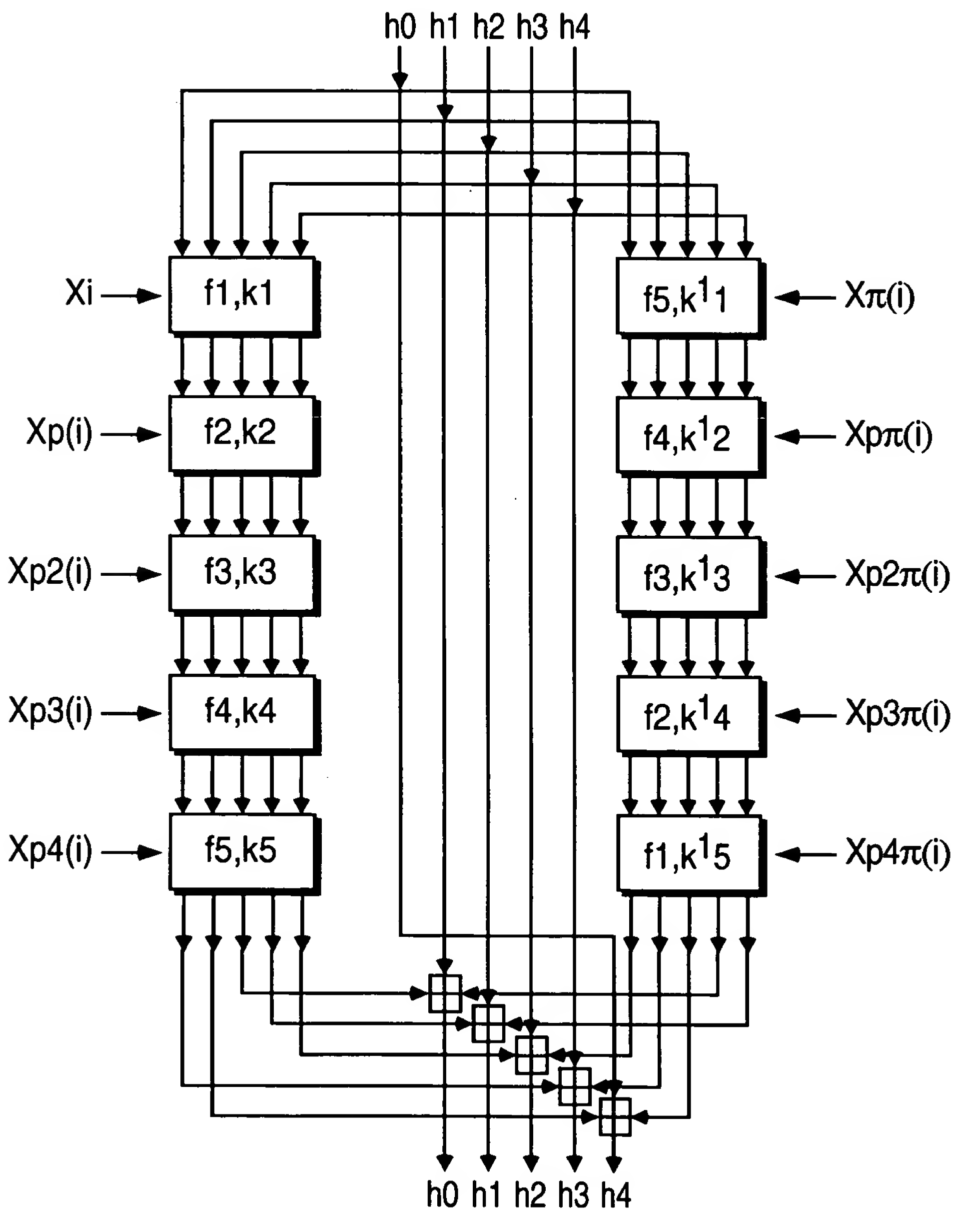


FIG. 67L

Outline of the compression function of RIPEMD-160.
Inputs are a 16 word message block Xi and a 5-word chaining variable h0h1h2h3h4, output is a new value of the chaining variable



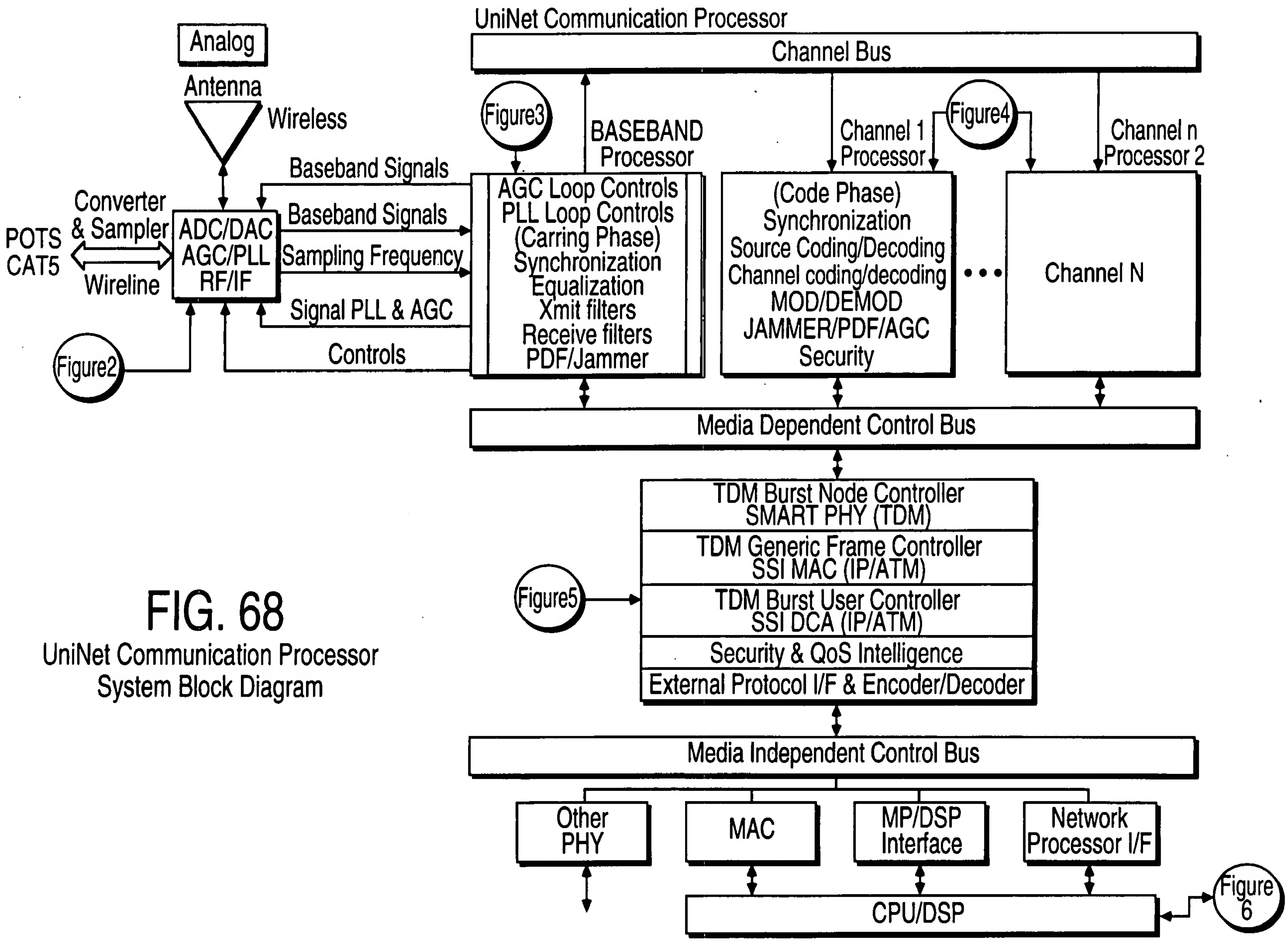


FIG. 68
UniNet Communication Processor
System Block Diagram

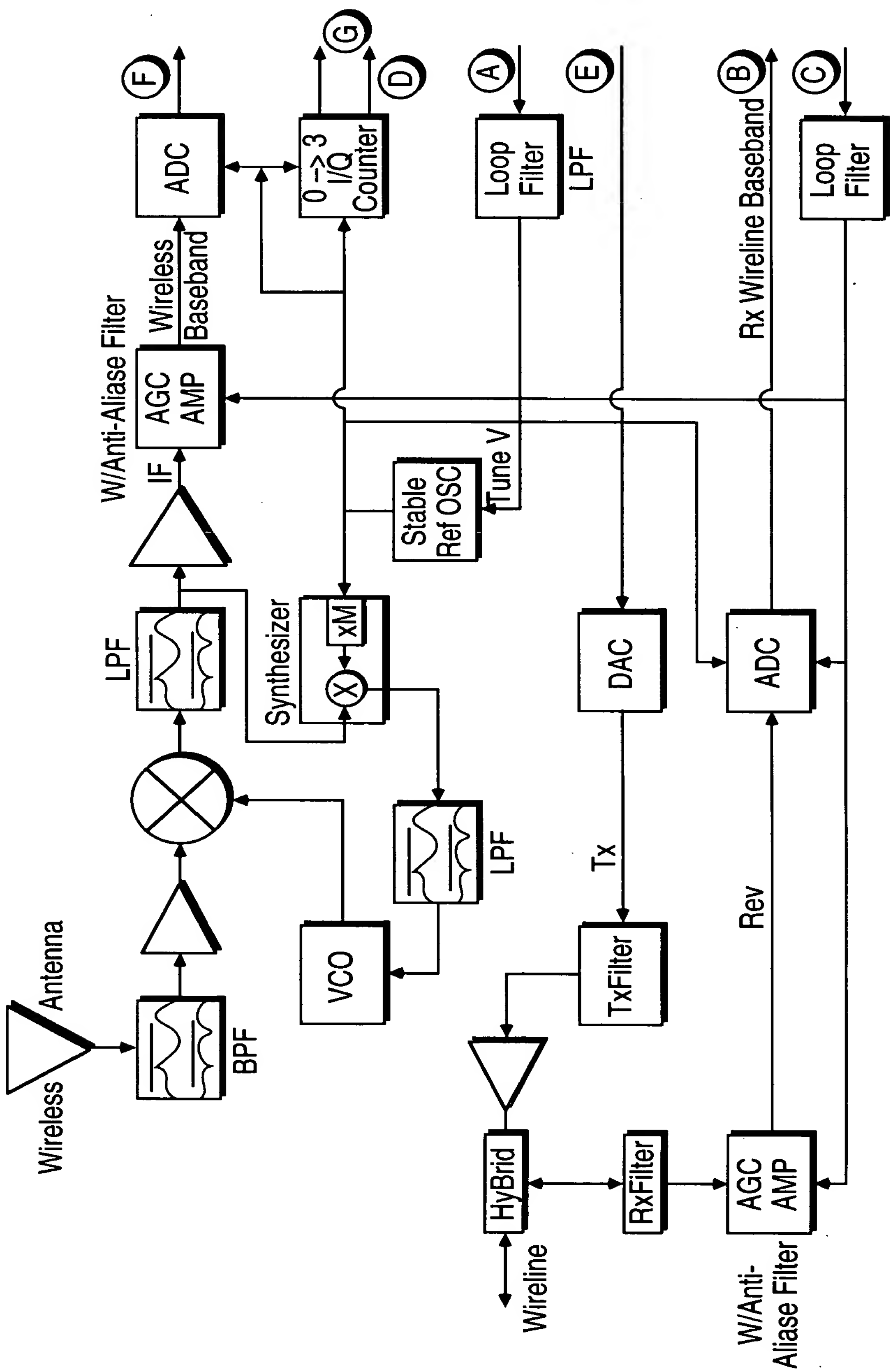


FIG. 69A
Baseband Converter and Sampler
(Receiver Only View for Wireless)

Title: "Channel Equalization System And Method"
Inventors: Francois Trans & Tho Le-Ngoc
Atty. Docket No.: 20870-06001; Case 6001 US
Application No.: Not Yet Known
Sheet 78 of 97

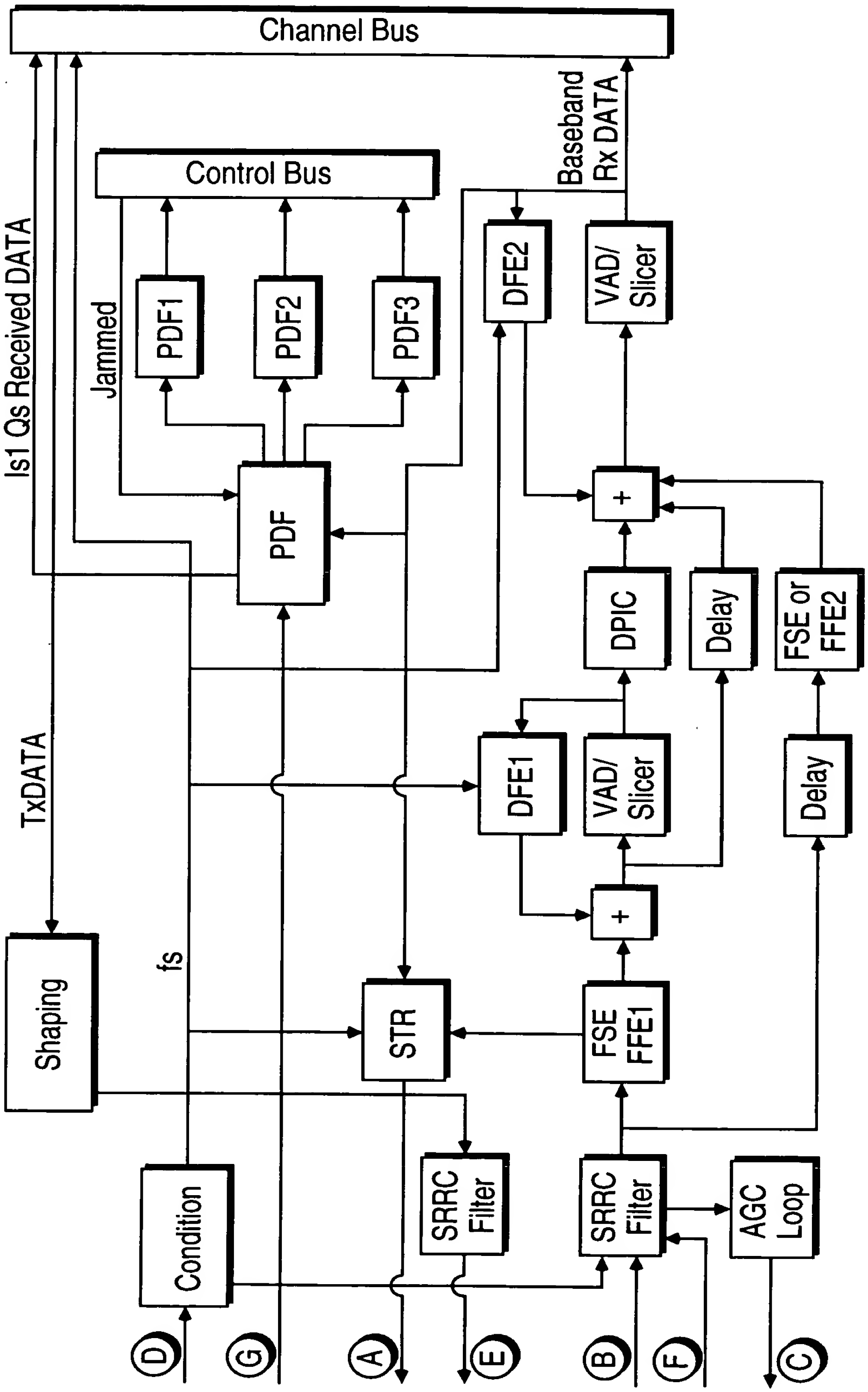


FIG. 69B
Baseband Processor

FIG. 70

PoR Prototype System for Applications using POTS as Communications Media

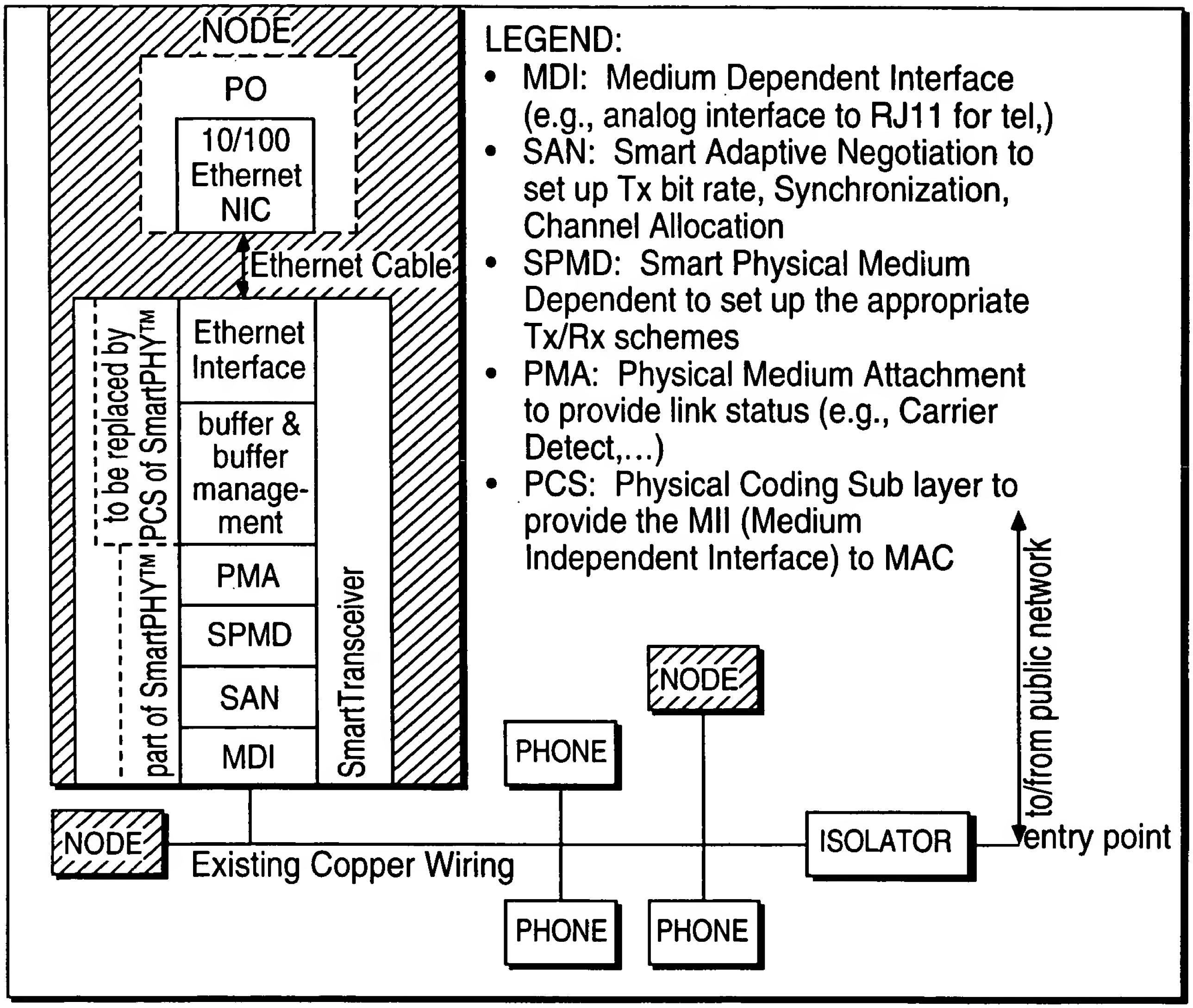


FIG. 71

Block Diagram of the Prototype

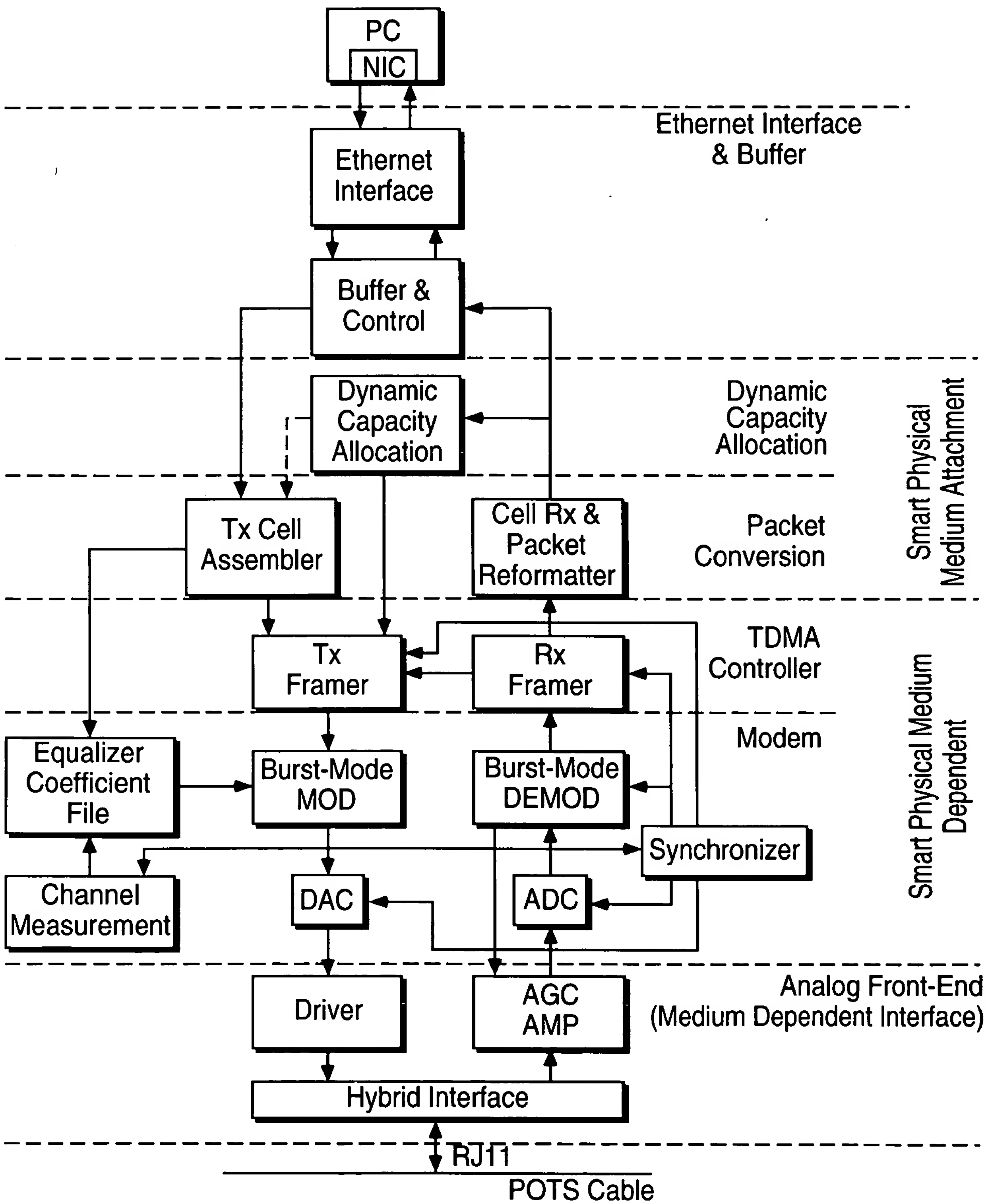
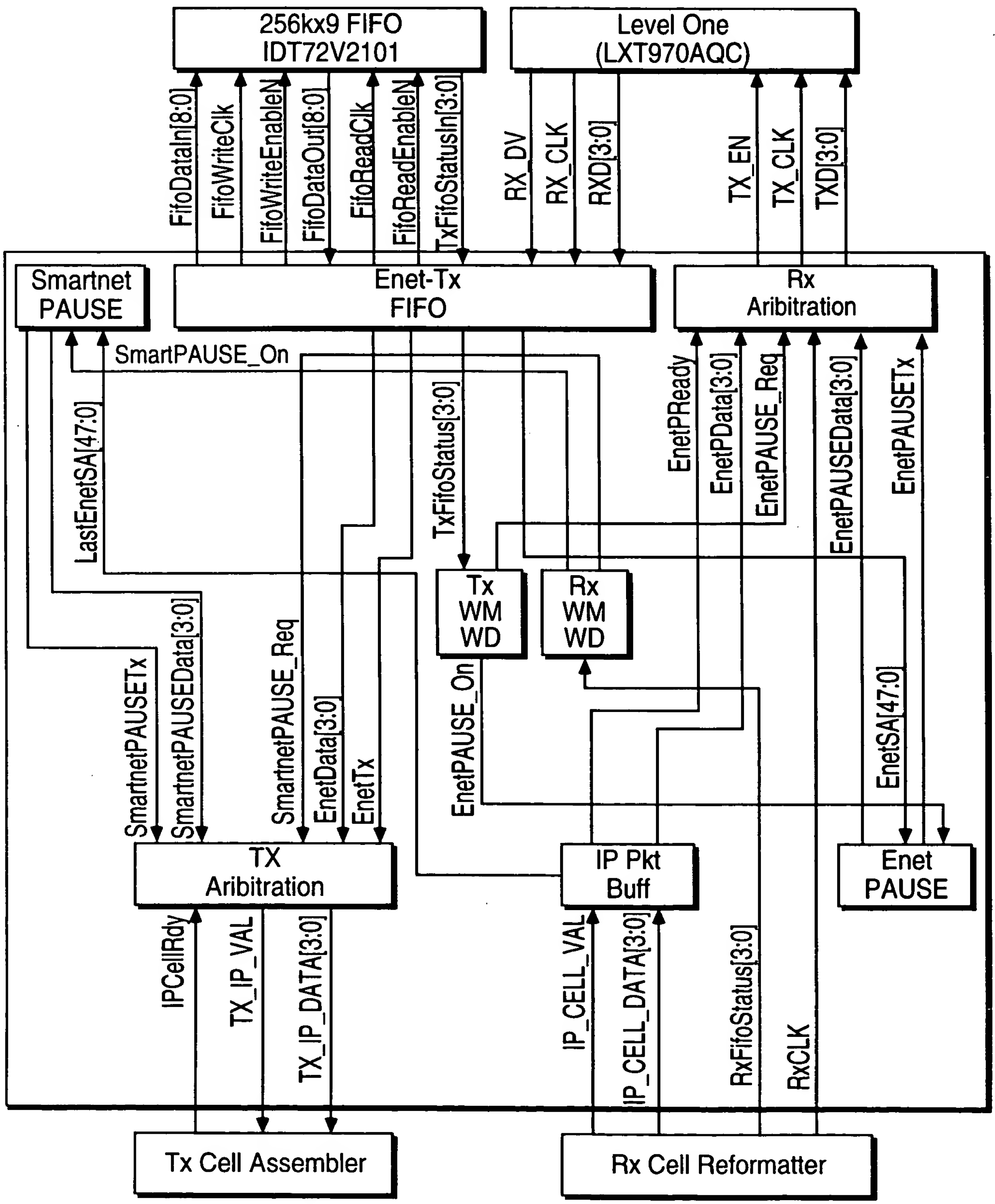


FIG. 72

Ethernet Interface and Buffer Management



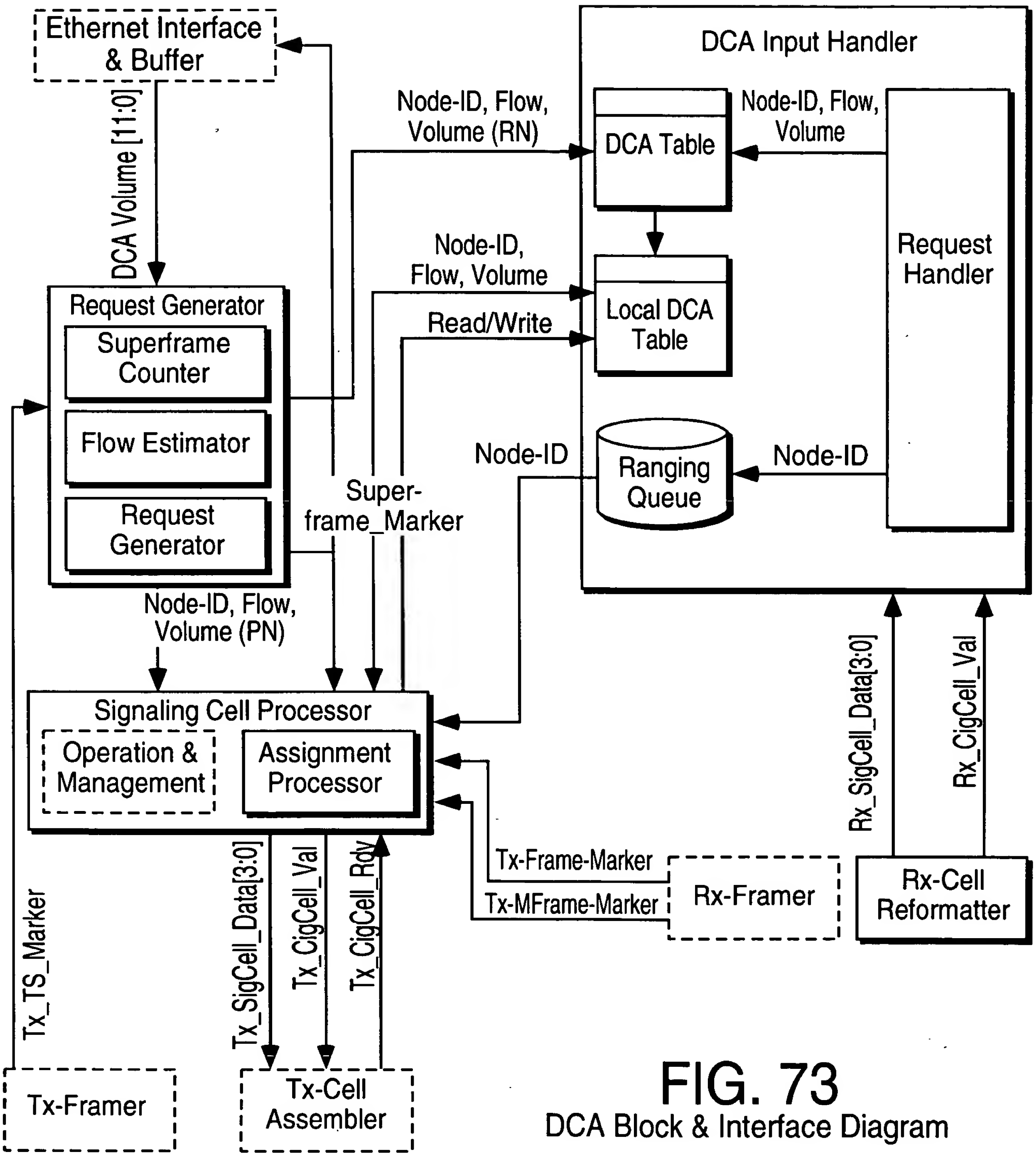


FIG. 73
DCA Block & Interface Diagram

FIG. 74

DCA Assignment Processes

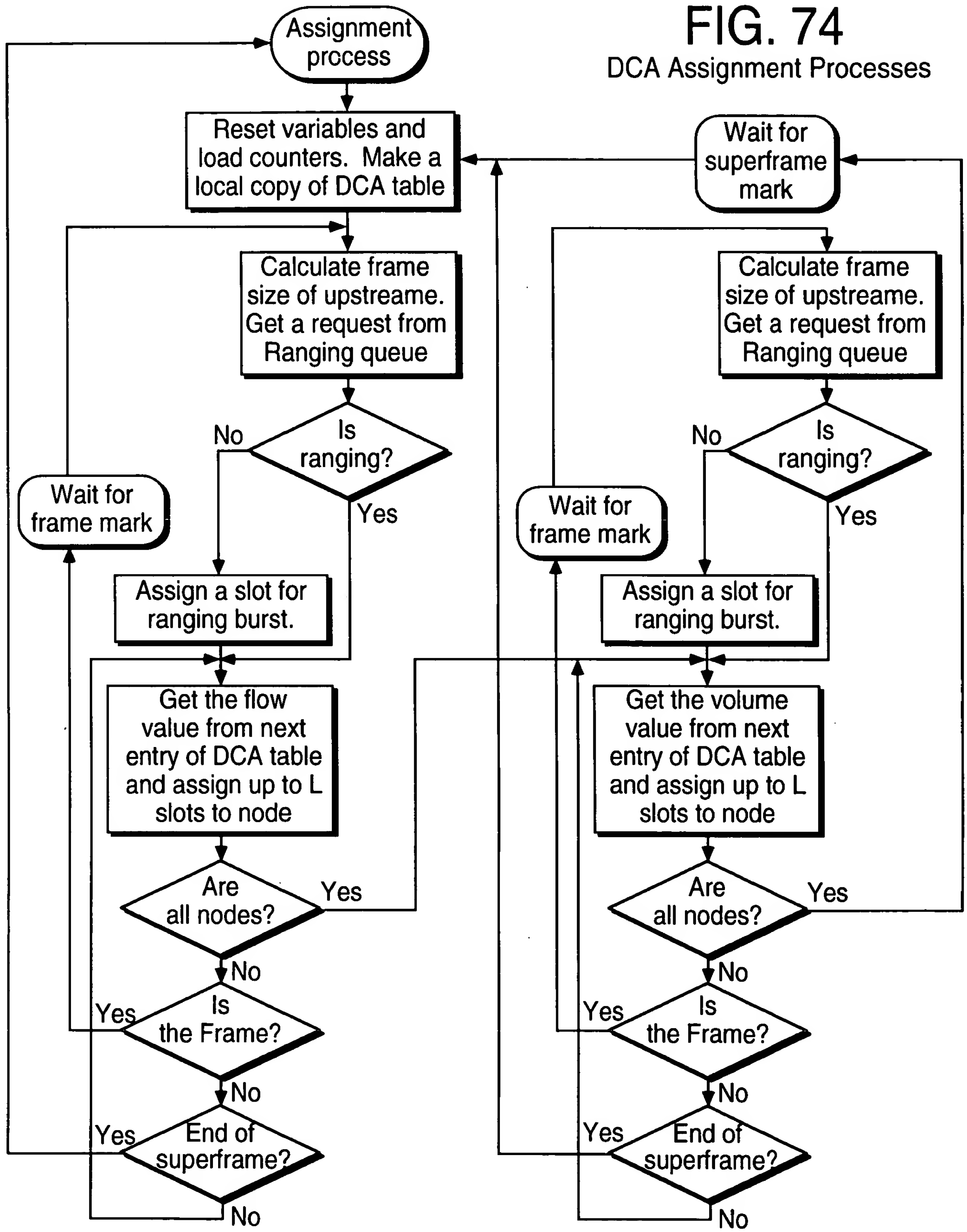
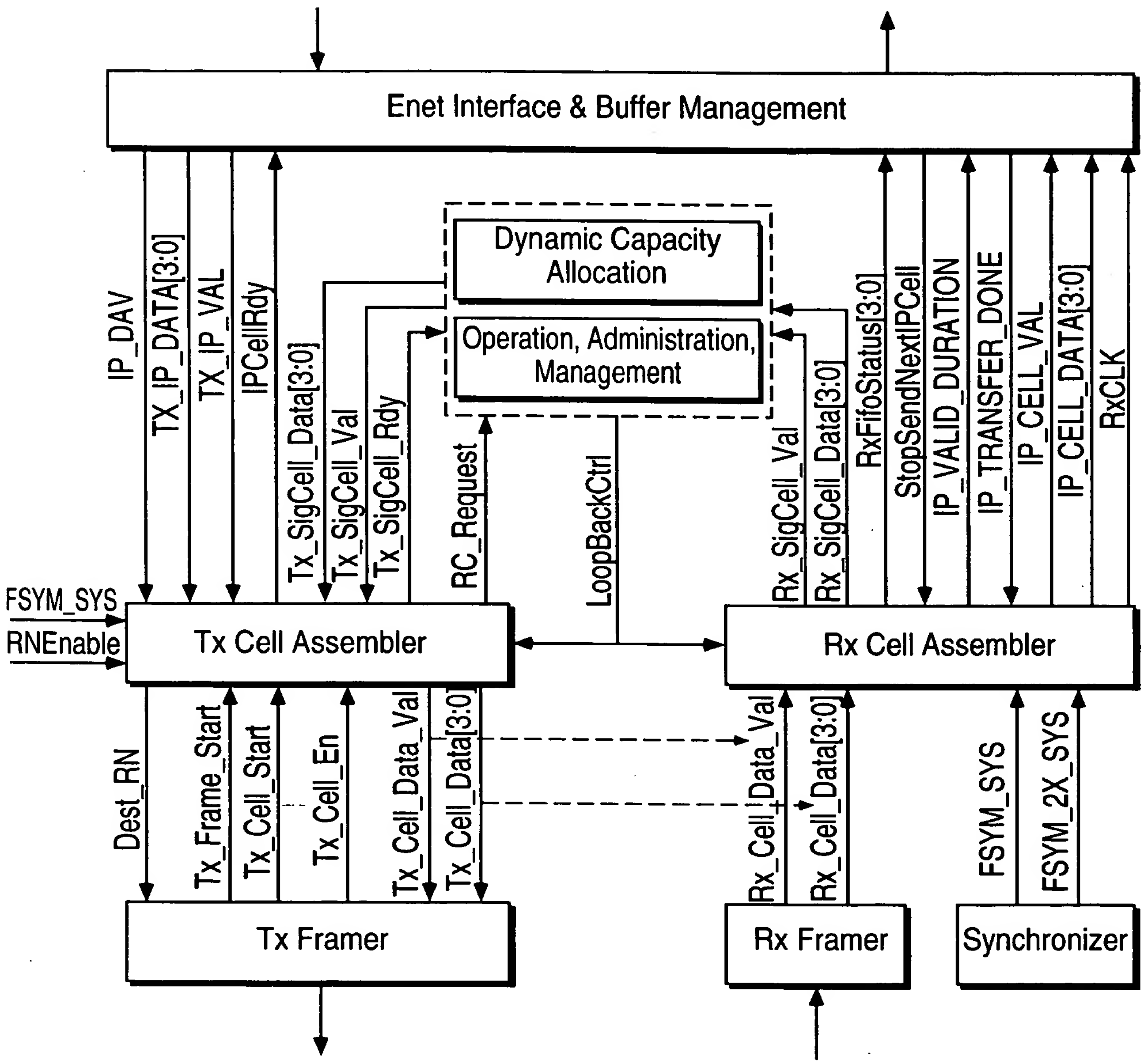


FIG. 75
Packetizer Block Diagram



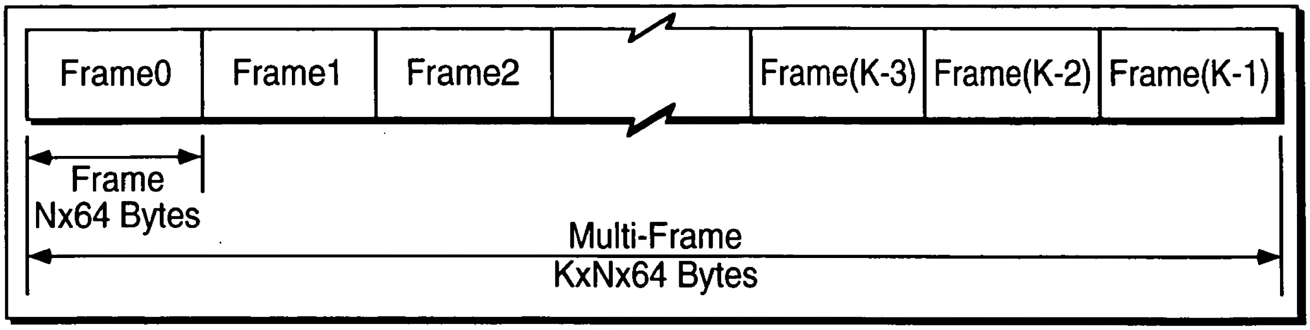


FIG. 76
Multi-Frame Format

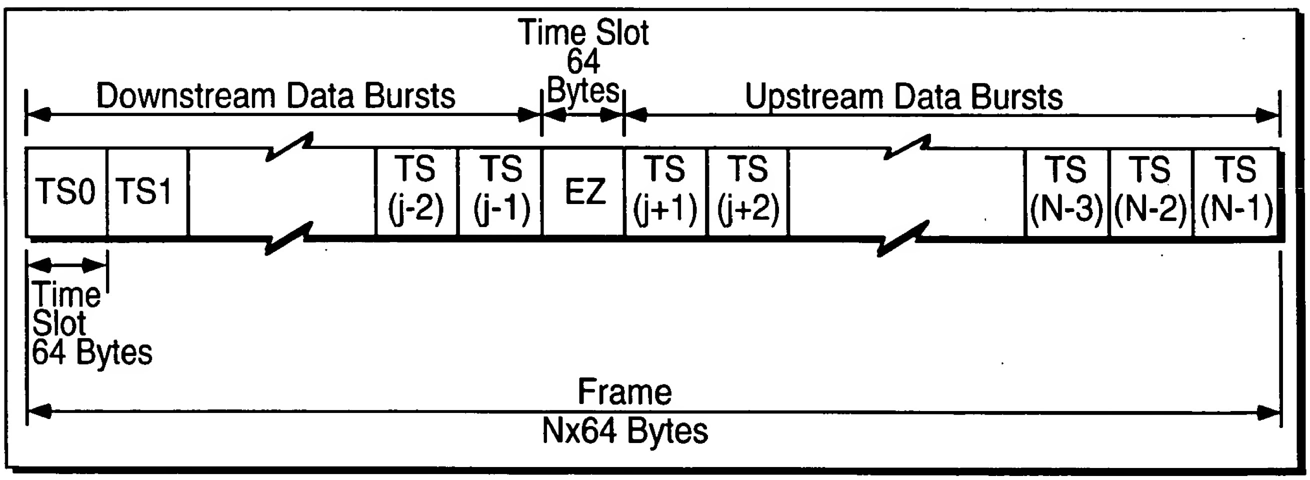


FIG. 77
Frame Format

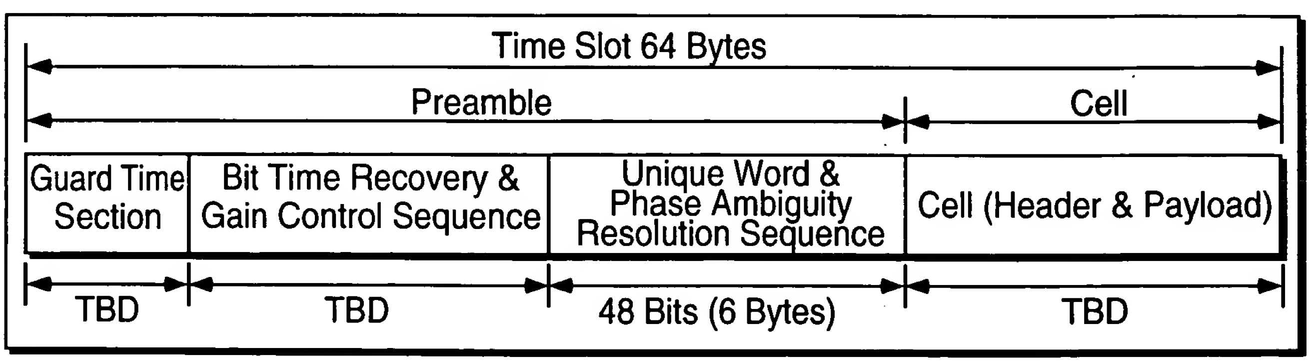


FIG. 78
Burst Format

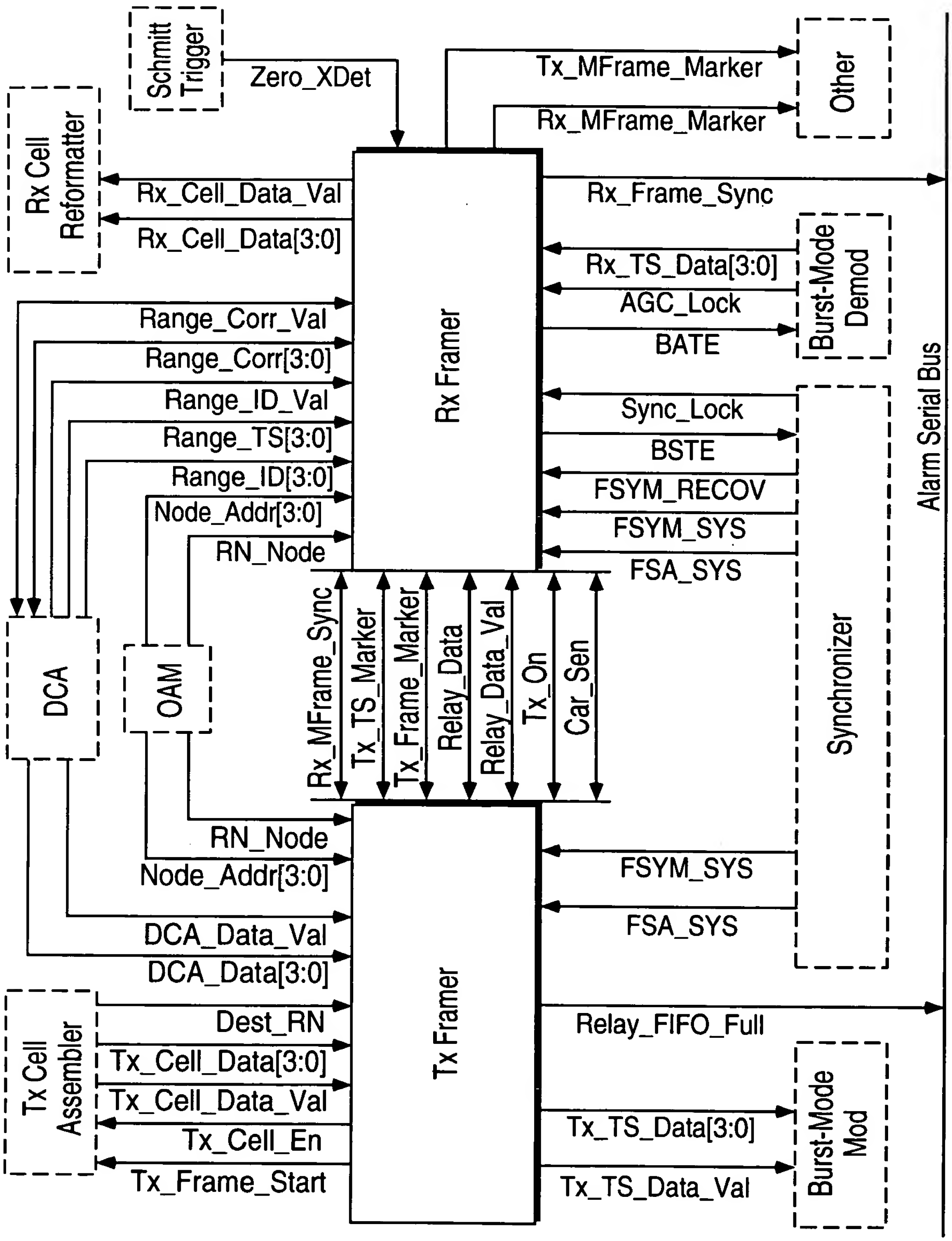


FIG. 79
TDMA Controller Interface

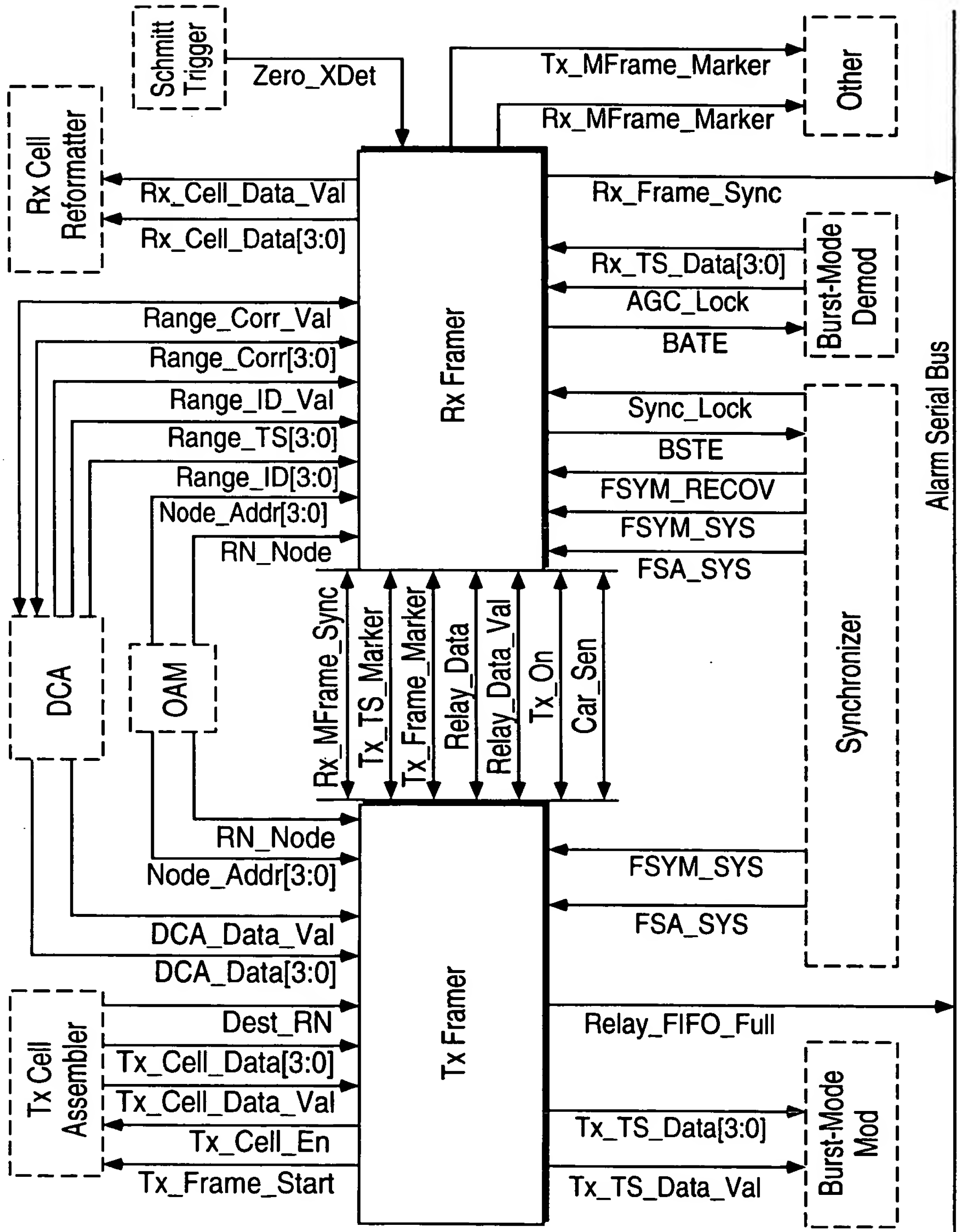


FIG. 80
TDMA Controller Interface

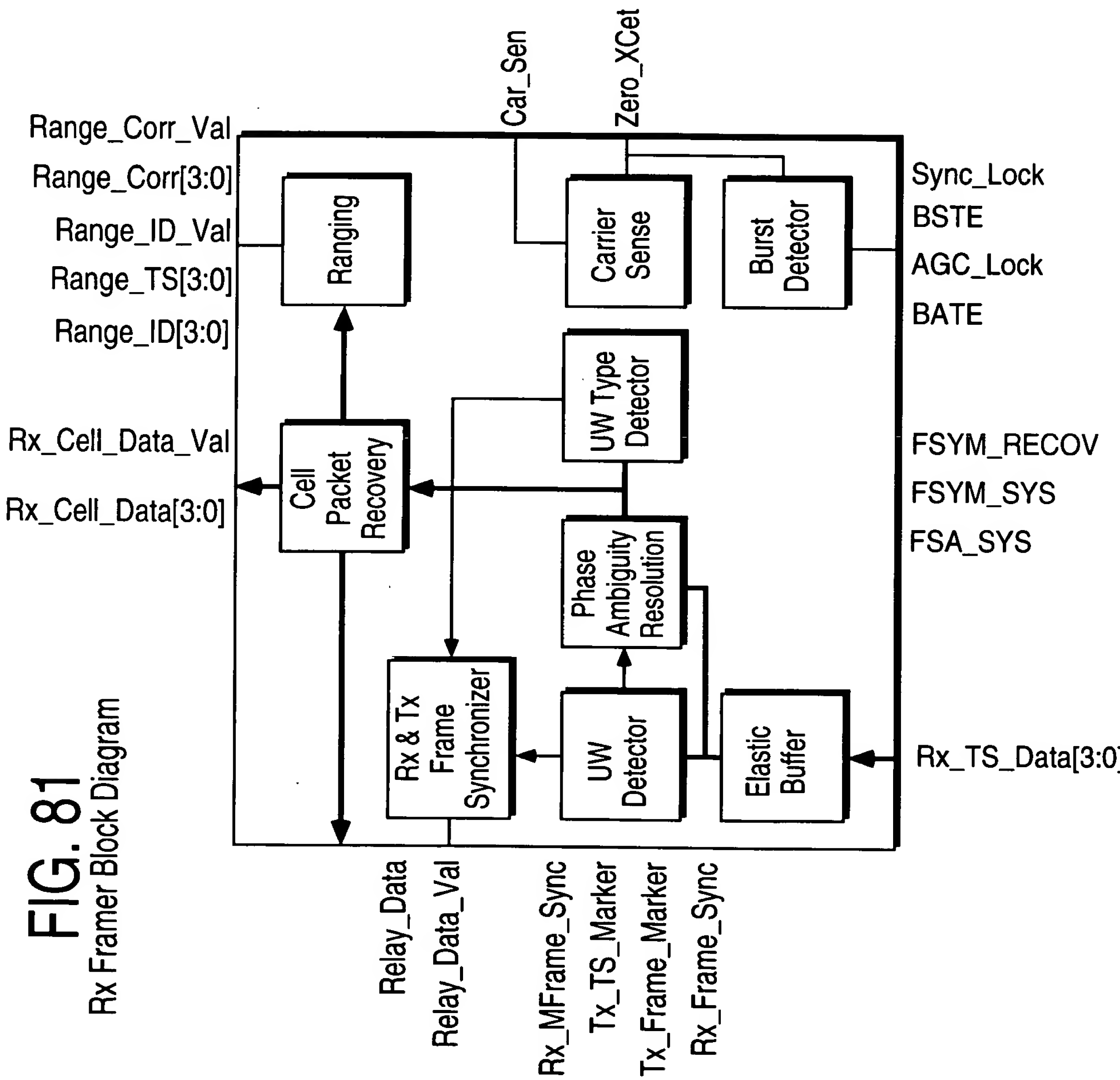
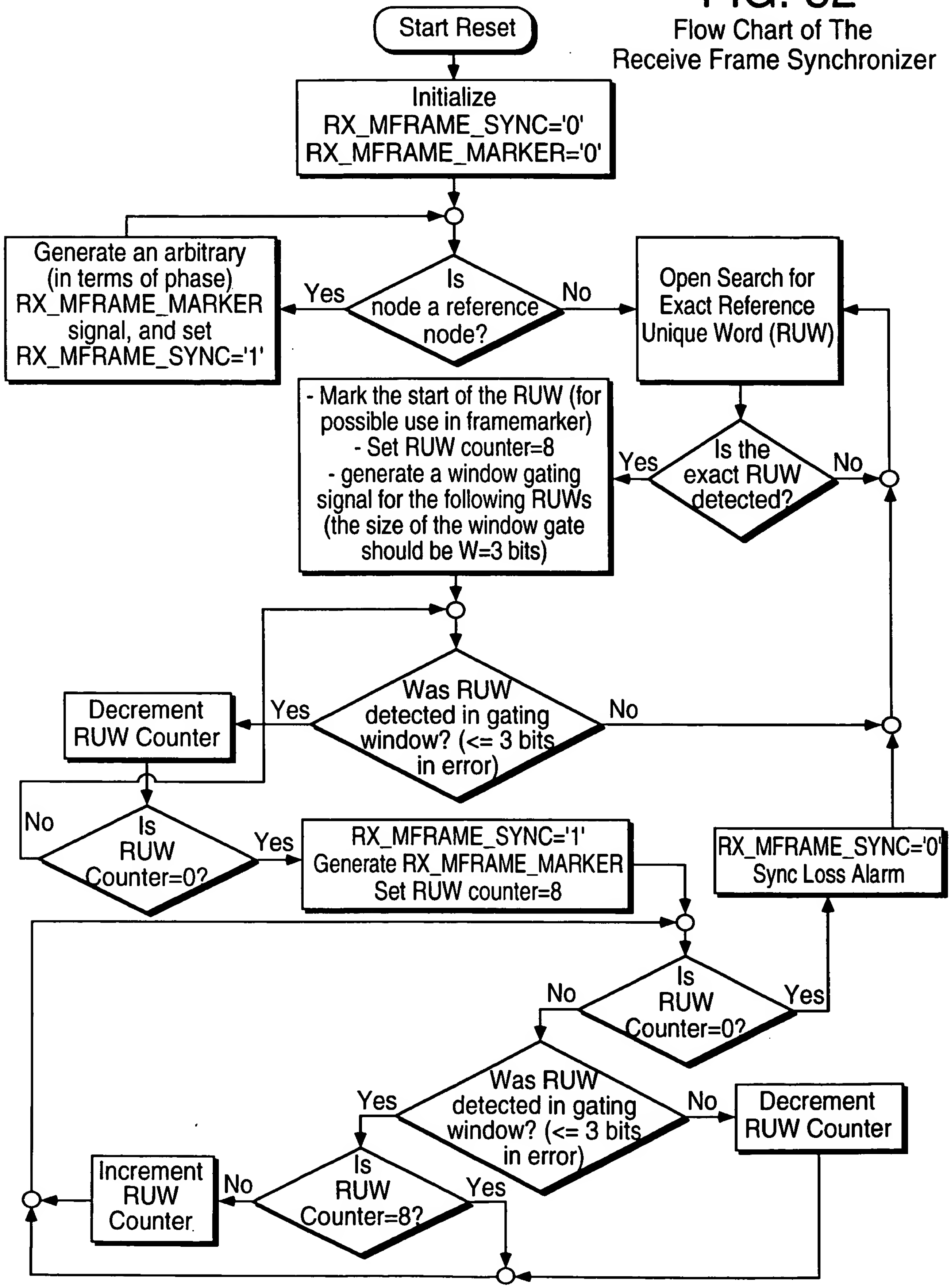


FIG. 81
Rx Framer Block Diagram

FIG. 82
Flow Chart of The Receive Frame Synchronizer



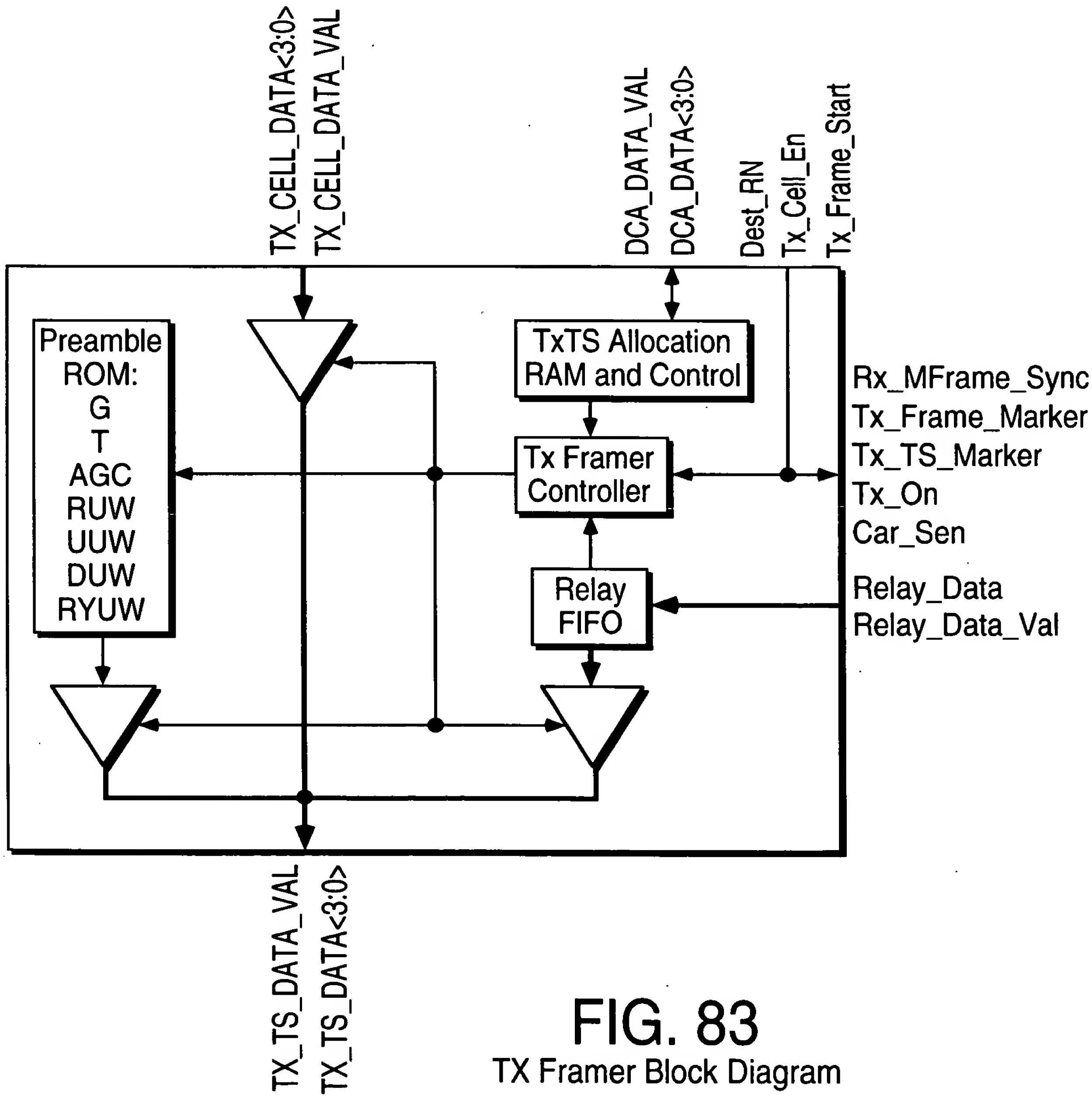


FIG. 83
TX Framer Block Diagram

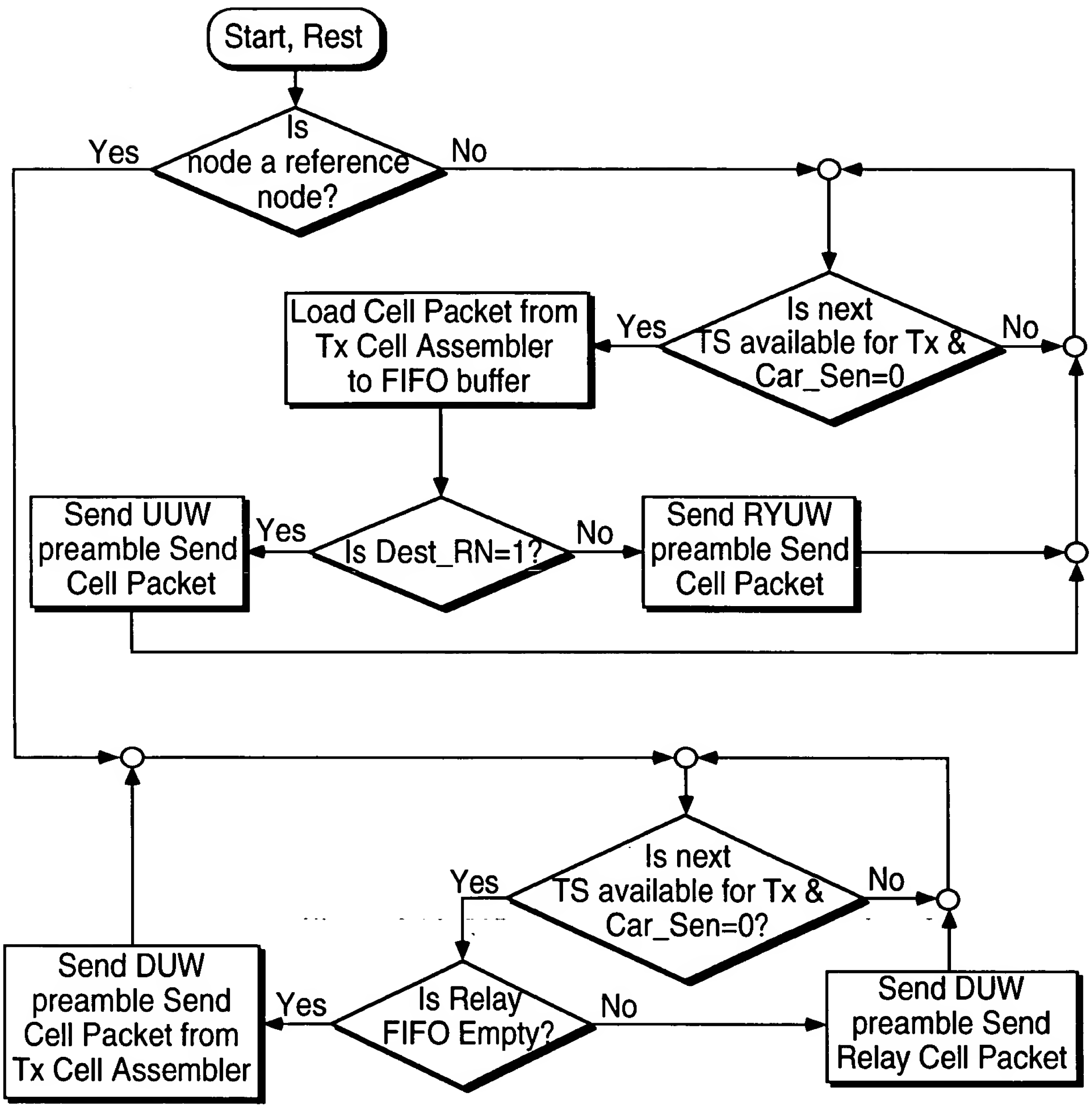


FIG. 84
TX Framer Controller

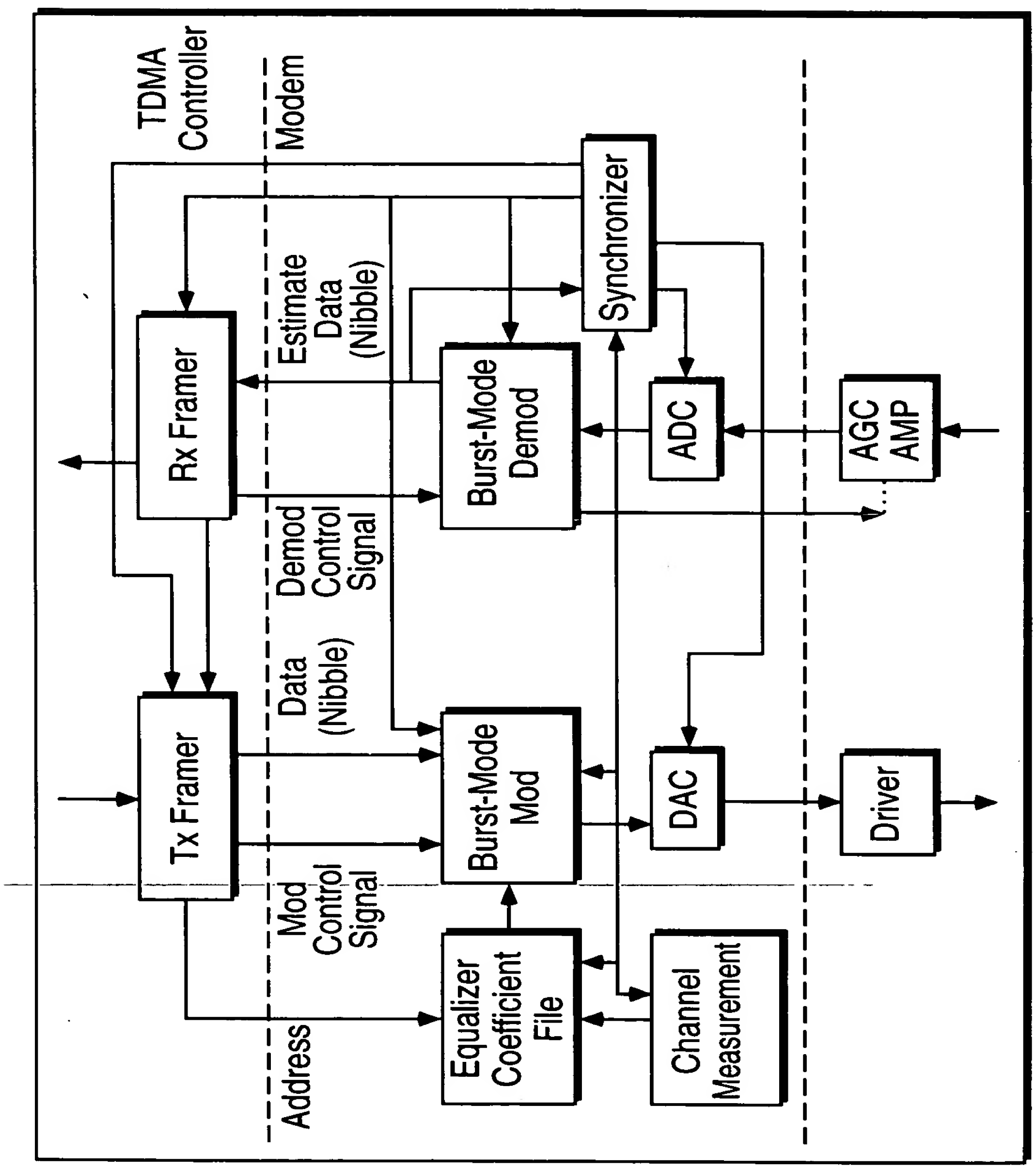


FIG. 85
Burst-Mode Modem Block Diagram

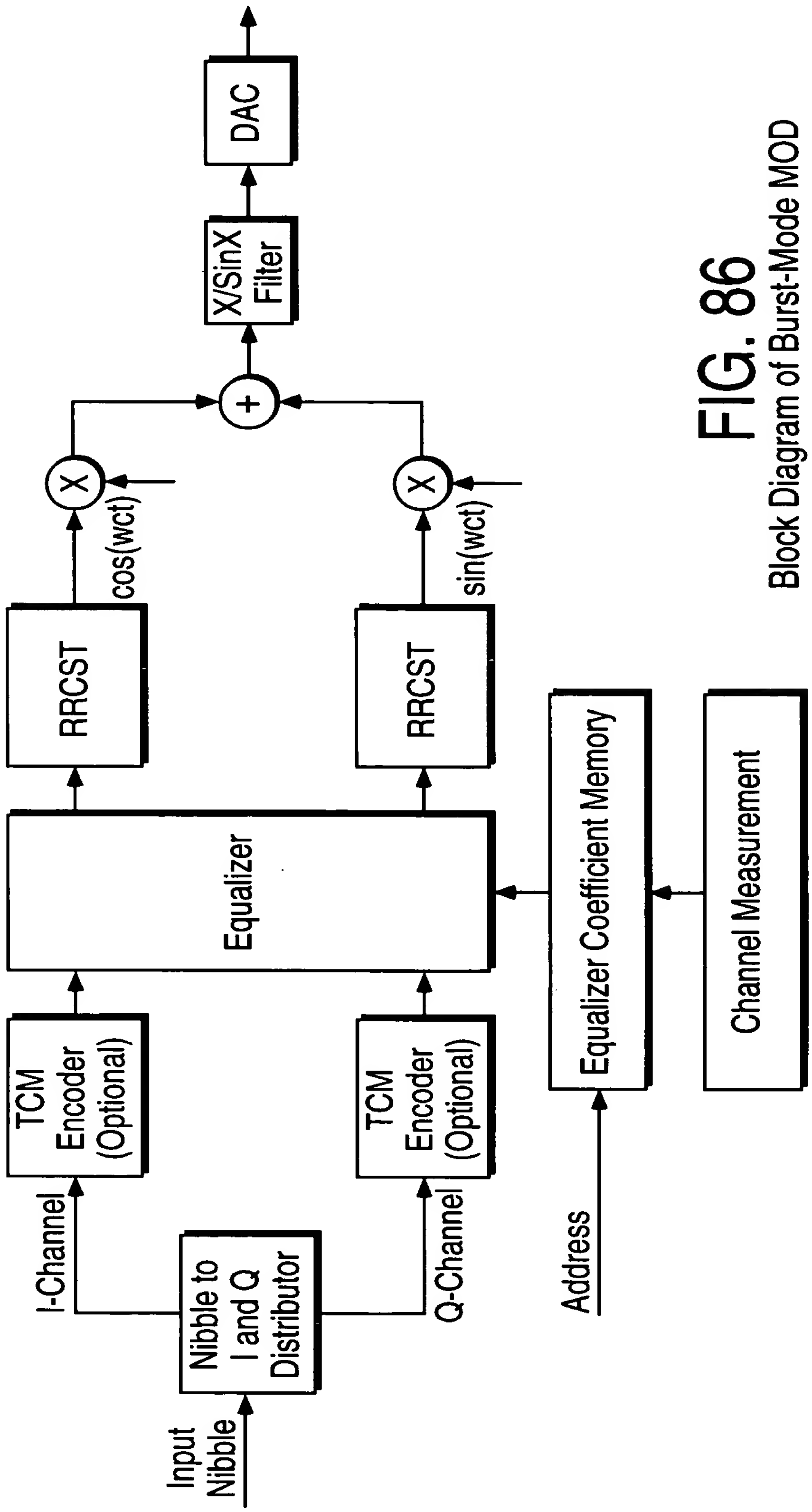


FIG. 86
Block Diagram of Burst-Mode MOD

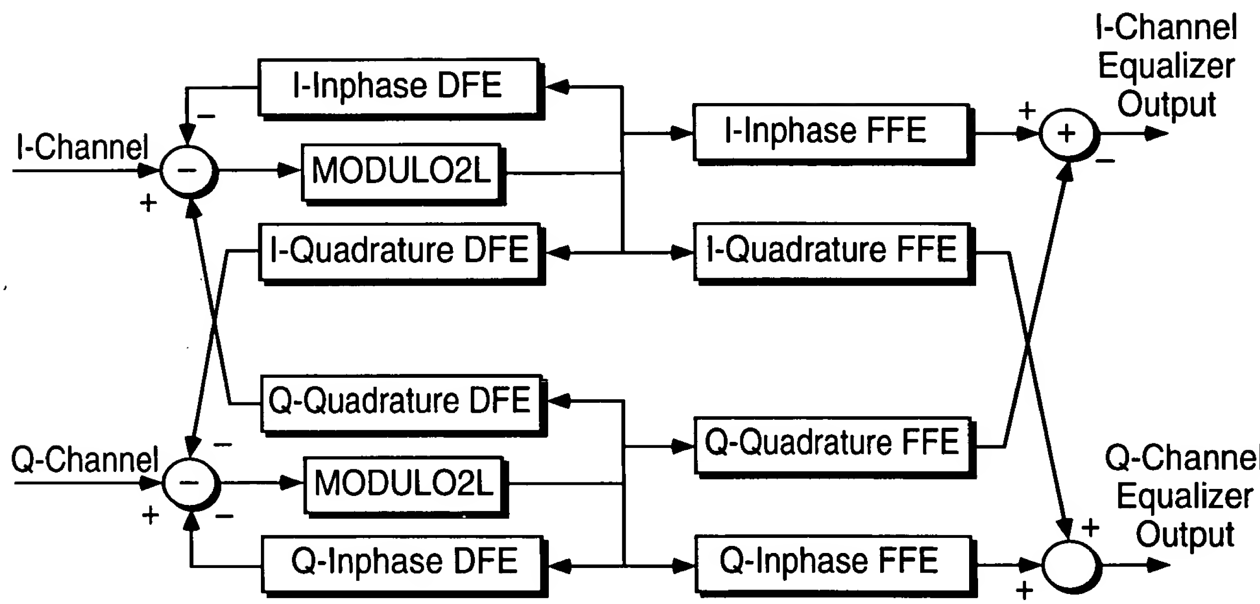


FIG. 87

Block Diagram of Equalizer

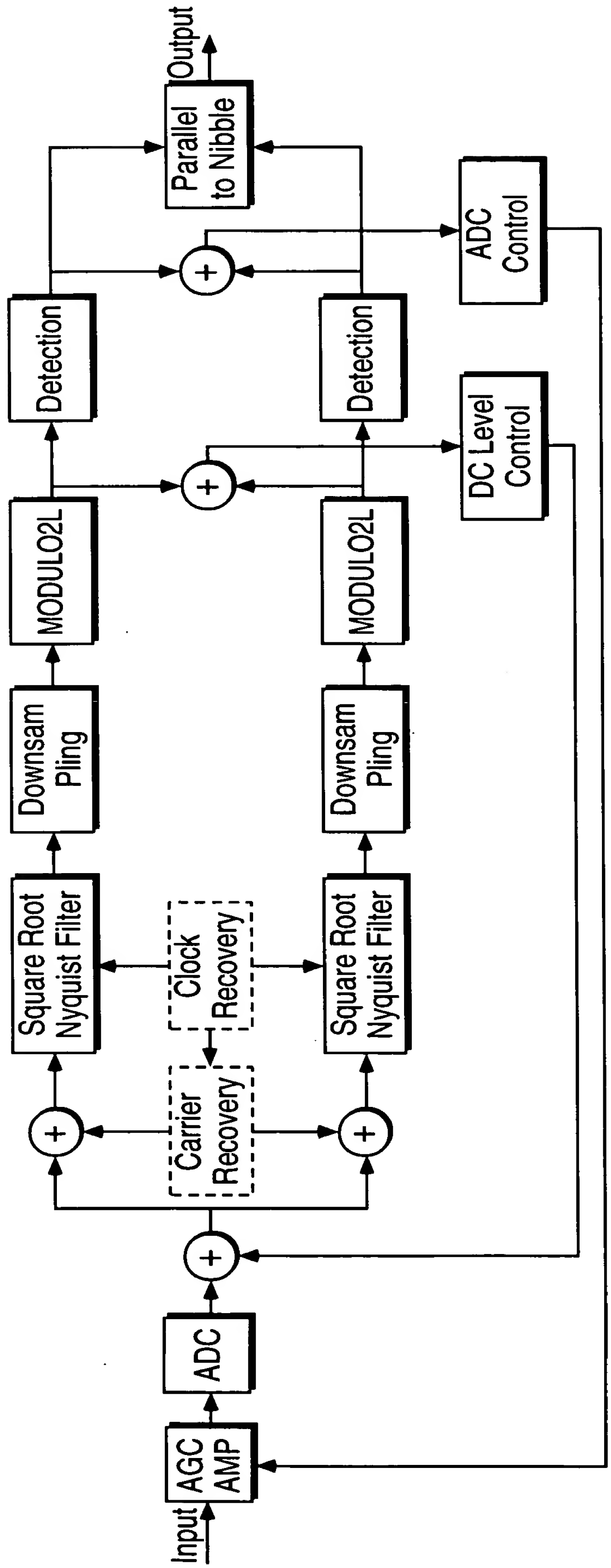


FIG. 88
Block Diagram of Burst-Mode DEMOD

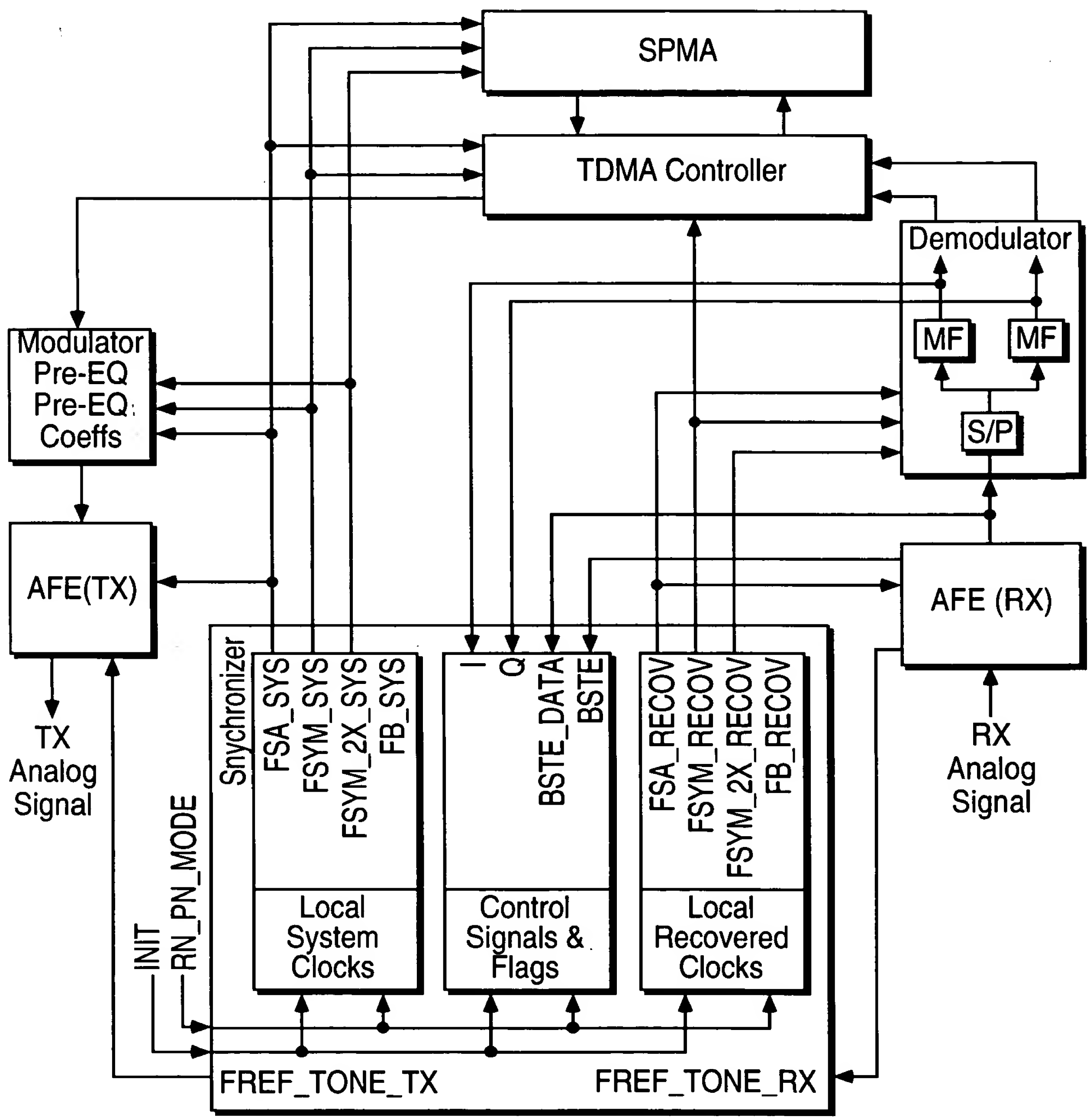


FIG. 89
Synchronizer Block & Interface Diagram

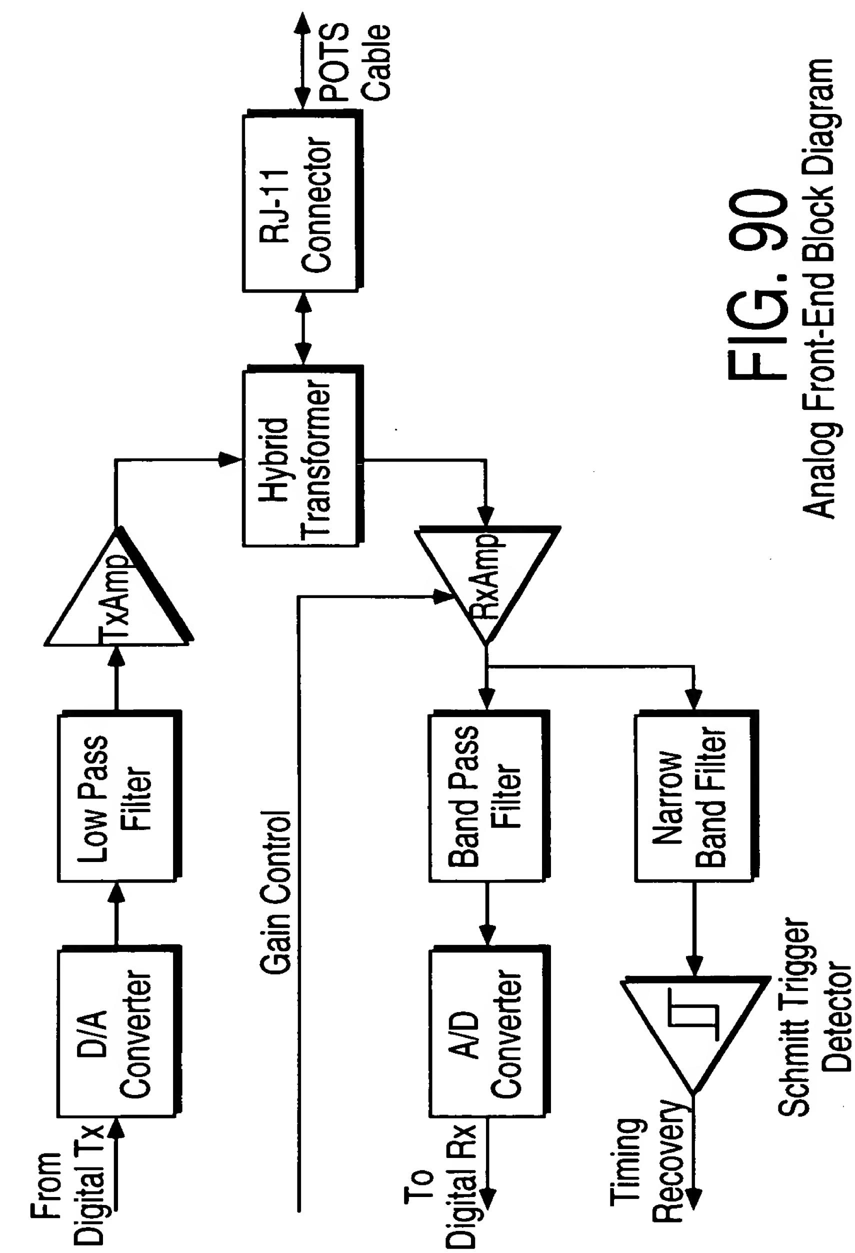


FIG. 90
Analog Front-End Block Diagram